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Subcontractor Report

Thin-Film Photovoltaic Partnership — CIS-Based Thin Film PV Technology

Final Technical Report
September 1995 — December 1998

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Siemens Solar Industries
Camarillo, California

National Renewable Energy Laboratory

1617 Cole Boulevard
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NREL Technical Monitor: H.S. Ullal

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Preface

Siemens Solar Industries (SSI) has pursued the research and development of $CuInSe_2$-based thin film PV technology since 1980 (1). SSI began a 3-year, 3 phase cost-shared subcontract (No. ZN-1-19019-5) on May 1, 1991 with the overall project goal of fabricating a large area, stable, 12.5% aperture efficient encapsulated CIS module by scaleable, low-cost techniques on inexpensive substrates. At the start of this subcontract SSI had demonstrated a 14.1% efficient 3.4 cm^2 active-area cell, unencapsulated integrated modules with aperture efficiencies of 11.2% on 940 cm^2 and 9.1% on 3900 cm^2, and an encapsulated module with 8.7% efficiency on 3883 cm^2 (verified by NREL). Subcontract accomplishments included demonstration of encapsulated module efficiencies that were at that time the highest reported mini-module efficiencies for any thin film technology (encapsulated 12.8% efficient mini-module on 68.9 cm^2 and an NREL-verified 12.7% efficient unencapsulated circuit on 69 cm^2 with a prismatic cover), demonstration of a champion large area (3860 cm^2) encapsulated module efficiency of 10.3% (verified by NREL) that was the first thin film module of its size to exceed the 10% efficiency level, and delivery to NREL of a one kilowatt array of large area (~3890 cm^2) approximately 30 watt modules (2).

The primary objective of this subcontract (#ZAF-5-14142-03) is to establish reliable high-throughput, high-yield thin film deposition processes in order to make CIS a viable option for the next generation of photovoltaics. The primary goals for the project are to deliver a champion prototype 13% efficient large area module and to deliver sets of modules in 1 kW arrays composed of steadily increasing efficiency, reaching 1 kW of 12% efficient large-area modules by the end of the third year, demonstrating performance as well as commercial viability. This focus on sets of high-performance modules as deliverables reflects SSI's commitment to demonstrating a reliable low-cost product. This document is the final subcontract report on progress toward these objectives and goals through the three-year period of this subcontract, September 1995 through December 1998.

Acknowledgments

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The Siemens Solar Industries CIS Team:

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Siemens Solar GmbH
Siemens AG

Summary

Multinary Cu(In,Ga)(Se,S)2 absorbers (CIS-based absorbers) are promising candidates for reducing the cost of photovoltaics well below the cost of crystalline silicon. The primary objective of this subcontract (#ZAF-5-14142-03) is to establish reliable high-throughput, high-yield thin film deposition processes in order to make CIS a viable option for the next generation of photovoltaics. The primary goals for the project are to deliver a champion prototype 13% efficient large area module and to deliver sets of modules in 1 kW arrays composed of steadily increasing efficiency, reaching 1 kW of 12% efficient large-area modules by the end of the third year, demonstrating performance as well as commercial viability. A major contract work theme is associated with each year, or phase, of this subcontract: Phase 1 - demonstration of reproducibility and yield for 10x10-cm mini-modules, Phase 2 - scale-up to large area substrates, and Phase 3 - demonstration of reproducibility and yield for large area modules. Outdoor testing, accelerated environmental testing, and packaging development progressed throughout all phases of this subcontract.

Demonstration of reproducibility and yield for 10x10-cm mini-modules was the main work theme for the Phase 1 of this subcontract (3, 4, 5, 6). From an industrial perspective, the full process sequence anticipated for use in the final product must be mastered and rigorously demonstrated. Statistical process control (SPC) techniques were applied to rigorously demonstrate yield and reproducibility. SSI abandoned development based on individual cells and defined a 10x10-cm monolithically interconnected "mini-module" baseline process that exercises all aspects of large area module production. During Phase 1, SSI repeatedly executed this baseline process, rigorously demonstrating process reproducibility and yield. SSI demonstrated an NREL confirmed 13.6% aperture area efficient mini-module .

Scale-up to large area substrates was the main work theme for the Phase 2 of this subcontract (7, 8). During Phase 2, SSI demonstrated that differences between baseline and large area absorber formation reactor designs were responsible for differences in absorber layer properties and cell performance. These differences were isolated to differences in the materials of construction and the physical design of the large reactor. As a result of these studies, and advances in understanding the influence of reactor design on performance, SSI designed and built a new large area reactor based on a more direct scale-up of the baseline reactor. Success with this development effort was first demonstrated by comparable performance for baseline mini-modules and 28x30-cm circuit plates. SSI also developed new products and prototype large area modules while building this new large area reactor. Circuit plates were fabricated using the baseline reactor that could only process small, ~10x30 cm, circuit plates. Modules were formed from these circuit plates using a newly developed package design to integrate small circuit plates into larger modules. SSI delivered a 1 kW array of $Cu(In,Ga)(S,Se)_2$ modules replacing the previously installed array which was based on an older absorber formation technology without sulfur incorporated in the absorber ($Cu(In,Ga)Se_2$). This array demonstrated significant improvements in efficiency and the temperature coefficient for power. SSI introduced two new 5 (ST5) and 10-watt (ST10) CIS-based products designed for use in 12 V systems, and NREL confirmed a new world-record efficiency of 11.1 percent on a SSI large area (3665 cm^2) module.

Demonstration of reproducibility and yield for large area modules was the main work theme for Phase 3 of this subcontract (9, 10, 11). During subcontract Phase 3, substrate size was scaled from ~30x30 cm to ~30x120 cm in the new large area reactor and all subsequent device formation processes. Fabrication of modules from ~10x30 cm circuit plates was discontinued and only ~30x120 cm circuit plates were used to make ~30x120 and smaller modules. Production of prototype ~30x120 cm circuit plates was conducted while applying SPC and Analysis of Variation methodologies to develop a low variation process through repeated “cycles of learning.” About 1300 ~30x120 cm circuit plates were produced

between January and November of 1998. The process exhibited generally good control for extended periods with an average efficiency of 10.8%. Periodic shifts in the short-term process average between about 10.25 and 11.25 are not yet understood but appear to result from batch-to-batch variability in precursor or base electrode preparation. Similarly, periodic shunting along the laser scribed pattern lines in the Mo base electrode appears to result from batch-to-batch variability in base electrode preparation. Mechanical yield, the fraction of all substrates introduced into production which pass intermediate inspections before IV testing, was 74%. Electrical yield depends upon the choice of lower specification limit; 85% yield at 10% minimum circuit efficiency and 96% yield at 9% minimum efficiency. Commercial product samples were delivered to NREL and a second set of ~30x120 cm modules (32 modules totaling ~1.2 kW) were delivered to the NREL Outdoor Test Facility. The NREL measured average efficiency at standard test conditions of 11.4% is the highest area efficiency for any thin-film technology and NREL confirmed a world-record 11.8% large area (3651 cm^2) efficiency for the champion module. The efficiency of all modules far exceeds the DOE year 2000 goal of 10% for commercial CIS modules.

Outdoor testing, accelerated environmental testing, and packaging development progressed throughout all phases of this subcontract. Approaches to package development during this subcontract were largely determined by requirements imposed by absorber formation development efforts, and the introduction of new products. Packaging designs that protect laminates from water vapor ingress during damp heat testing have been demonstrated and multiple prototype module designs have passed accelerated tests, including the 1,000 hour, 85°C, 85% relative humidity damp heat test. However, thermally induced transient effects confound efforts to quantify the relative quality of alternative package designs and these effects have not been eliminated, the yield for passing the damp heat test with newly developed packages is typically low, and improved package designs are needed to meet the DOE long-term goal of "systems that last at least 30 years." Transient effects received significant consideration during this subcontract since transient effects are important for many topics in addition to accelerated testing: process definition, measurement protocols, process predictability, interpretation of experimental results, and understanding of device structures. Long-term outdoor stability has been demonstrated at NREL where 1x1 ft. and 1x4 ft. modules have undergone testing for as long as ten years. Measurements on both modules and 1kW arrays indicate good stability with no seasonal variation in performance. This demonstrates that thermally induced transients observed after exposure to accelerated environmental testing are not observed in the field despite daily and seasonal changes in module temperature.

Challenges remain to scale the process to larger substrates and higher capacity, and to pass accelerated environmental testing. The origin of thermal transient behavior needs to be identified and eliminated if possible. A package design needs to be developed to pass standard environmental qualification testing. The outstanding progress toward achieving NREL/DOE goals achieved during this subcontract demonstrates that CIS is a viable option for the next generation of photovoltaics.

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Introduction

Overview

Multinary $Cu(In,Ga)(Se,S)_2$ absorbers (CIS-based absorbers) are promising candidates for reducing the cost of photovoltaics well below the cost of crystalline silicon. CIS champion solar cells have exceeded 17% efficiency for devices fabricated at NREL (12). Small area, fully integrated modules exceeding 13% in efficiency have been demonstrated by several groups (13). Long-term outdoor stability has been demonstrated at NREL by ~30x30 cm and ~30x120 cm SSI modules which have been in field testing for as long as ten years (14). Projections based on current processing indicate production costs well below the cost of crystalline silicon (13).

Compared to traditional wafer-based crystalline silicon technologies, new thin film technologies yield products of comparable performance but with significant advantages in manufacturing (13):

- Lower consumption of direct and indirect materials
- Fewer processing steps
- Easier automation

Lower consumption of direct and indirect materials results in part from the thin-film structure (discussed below) for the semiconductor used to collect solar energy. All three of these manufacturing advantages are in part due to an integrated, monolithic circuit design illustrated in Figure 1. Unlike wafer-based technologies, monolithic integration eliminates multiple process steps that are otherwise required to handle individual wafers and assemble individual solar cells into the final product.

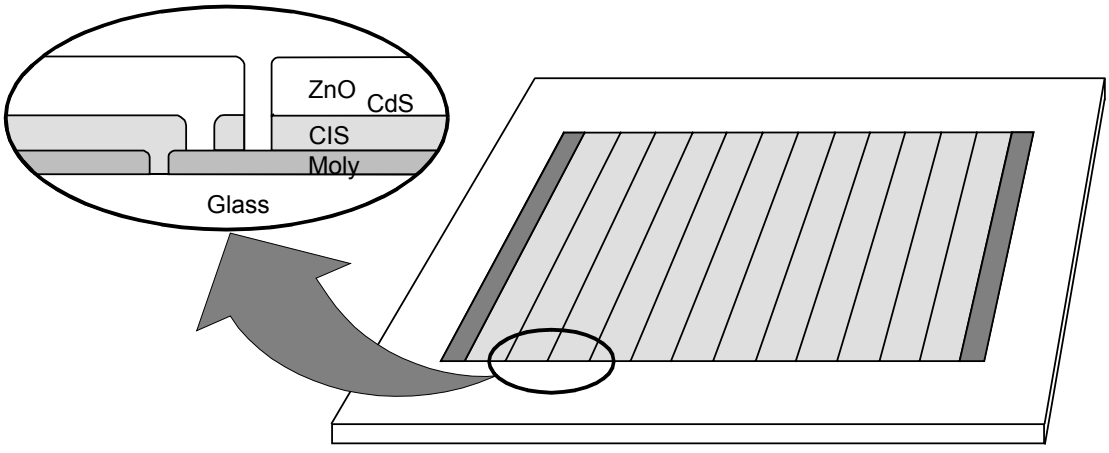


Figure 1. Structure of SSI's monolithically integrated thin-film circuits.

A number of thin film photovoltaic technologies have been developed as alternatives to the traditional solar cells based on crystalline silicon wafers (13). Those technologies with the greatest potential to significantly reduce manufacturing costs are based on alloys of amorphous silicon (a-Si), cadmium

telluride (CdTe), CIS, and film silicon (Si-film). These photovoltaic thin film technologies have similar manufacturing costs per unit area since all share common elements of design and construction:

- Deposition of typically three layers on a suitable substrate – window/electrode, absorber, and back electrode
- Patterning to create monolithically integrated circuit plates
- Encapsulation to construct modules

Cost per watt is a more appropriate figure of merit than cost per unit area (13). As discussed above, all thin film technologies have similar manufacturing costs per unit area since they all use similar deposition, patterning, and encapsulation processes. About half of the total module cost – material, labor, and overhead – originates in the encapsulation scheme which is for the most part independent of the thin film technology. Costs for alternative encapsulation schemes are typically similar or even higher. The average efficiency of large, ~30x120 cm modules in pilot production at Siemens Solar is nearly 11%. This performance is comparable to many modules based on crystalline silicon, and is substantially better than the performance reported for competing thin-film technologies. The lowest cost per peak watt will result from the technology with the highest efficiency, CIS technology, since most thin film technologies have similar cost per unit area.

SSI CIS Process

Most terrestrial photovoltaic products today are designed to charge a 12-volt battery, however the output voltage of an individual solar cell is typically about 0.5 volts. Wafer-based technologies build up the voltage by connecting individual solar cells in series. In contrast, CIS circuits are fabricated monolithically (Figure 1); the interconnection is accomplished as part of the processing sequence to form the solar cell by alternately depositing a layer in the cell structure and patterning the layer using laser or mechanical scribing.

The structure of a SSI CIS solar cell is shown in Figure 2. The full process to form CIS circuit plates, including monolithic integration, is outlined in Figure 3. This process starts with ordinary sodalime window glass, which is cleaned and prepared for the deposition of the thin films. A molybdenum (Mo) base electrode is sputtered onto the substrate. This is followed by the first patterning step (referred to as "P1") required to create monolithically integrated circuit plates – laser scribing to cut an isolation scribe in the Mo electrode. Copper and indium precursors to CIS formation are then deposited by sputtering. CIS formation is typically accomplished by heated the precursors in H_2Se and H_2S to form the CIS absorber. This deposition of copper and indium precursors followed by reaction to form CIS is often referred to as the two-stage process. A very thin coating of cadmium sulfide (CdS) is deposited by chemical bath deposition (CBD). This layer is often referred to as a "buffer layer." A second patterning step (P2) is performed by mechanical scribing through the CIS absorber to the Mo substrate thereby forming an interconnect via. A transparent contact is made by chemical vapor deposition (CVD) of zinc oxide (ZnO). This layer is often referred to as a "window layer" or a transparent conducting oxide (TCO). Simultaneously, ZnO is deposited on the exposed part of the Mo substrate in the interconnect via and thereby connects the Mo and ZnO electrodes of adjacent cells. A third and final patterning step (P3) is performed by mechanical scribing through the ZnO and CIS absorber to isolate adjacent cells.

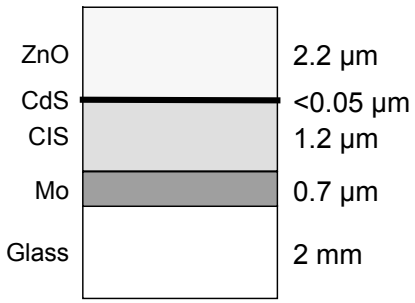


Figure 2. Structure of a SSI's CIS cell structure.

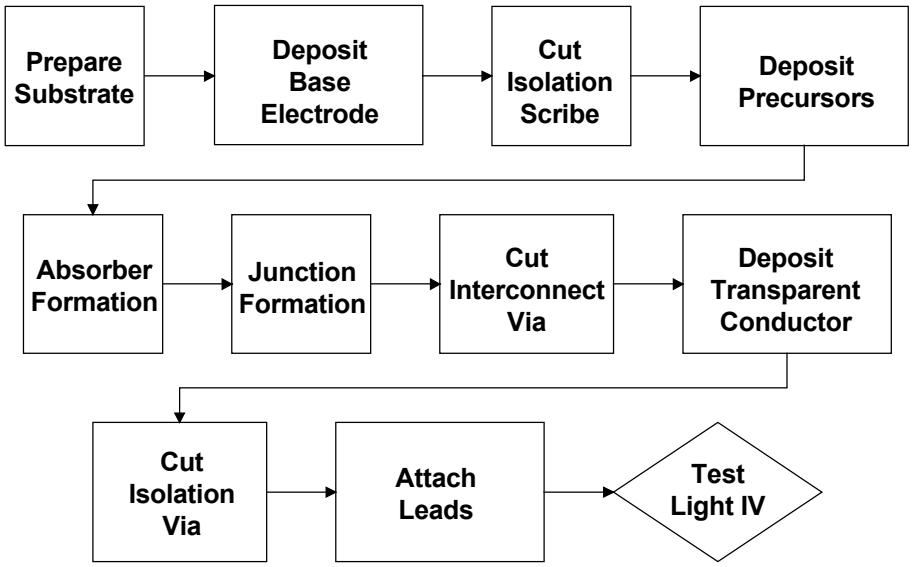


Figure 3. SSI CIS Circuit Processing Sequence.

The CIS-based absorber referred to in this report is composed of the ternary compound $CuInSe_2$ combined with sulfur and gallium to form the multinary compound $Cu(In,Ga)(S,Se)_2$. Gallium and sulfur are not uniformly distributed throughout the absorber but the concentrations are graded; hence, this structure is referred to as a "graded absorber." The graded absorber structure is a graded $Cu(In,Ga)(Se,S)_2$ multinary with higher sulfur concentration at the front and back and higher Ga concentration at the back. Elemental profiles typical of the SSI graded absorber structures are presented in Figure 4. Efficiency, voltage and adhesion improvements have been reported for the SSI graded absorber structure (2, 15, 16).

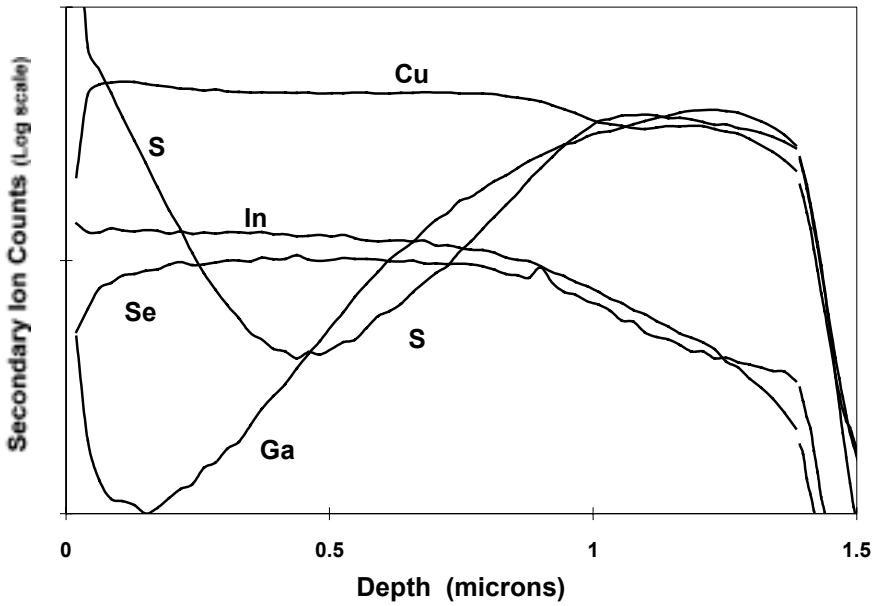


Figure 4. Typical elemental profile for the SSI graded absorber (SIMS from NREL).

This graded absorber structure is distinct from an absorber structure with a nearly uniform gallium or sulfur concentration throughout the absorber, although both types of structure may improve device efficiency. Based on a simple model, uniform increases in absorber bandgap should result in increases in device voltages at the expense of reduced current. The increase in voltage with increasing bandgap is due primarily to an increased built in voltage while the decrease in current is due to little absorption for photons with energies less than the bandgap energy. This tradeoff between voltage and current leads to

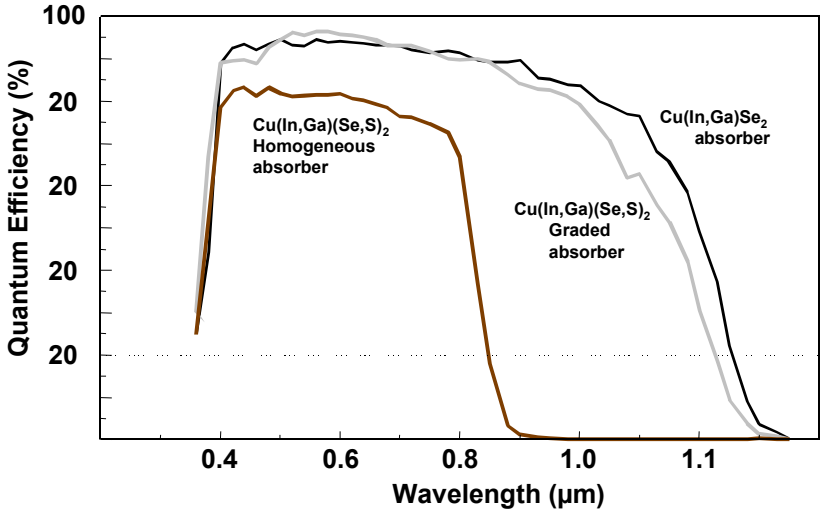


Figure 5 Spectral response for absorbers composed of homogeneous and graded Cu(In,Ga)(S,Se)2 multinary compounds.

the prediction of higher efficiency for bandgaps above the 1.0 eV bandgap of the $CuInSe_2$ compound up to about 1.5 eV. Although this increase in efficiency for higher bandgaps is significant for the ideal device model that assumes Auger recombination limits performance, the increase in efficiency is relatively modest for more realistic models based on recombination limited device performance. Uniform addition of sulfur or gallium to form a multinary compound increases the bandgap of the multinary compound relative to the bandgap of the ternary $CuInSe_2$ compound. In contrast, concentrations of sulfur and gallium are low in the center of the graded absorber structure, and the bandgap near the center of a graded absorber structure is not significantly shifted from the bandgap of the ternary $CuInSe_2$ compound. Quantum Efficiency for absorbers composed of homogeneous and graded $Cu(In,Ga)(S,Se)_2$ multinary compounds (Figure 5) illustrates that relatively long wavelength photons are not absorbed by a homogeneous multinary absorber whereas the long wavelength energy is only reduced for a graded absorber structure.

In addition to improving efficiency at standard test conditions, the counter variation of open circuit voltage with short circuit current due to the addition of sulfur and gallium can improve efficiency for fully integrated modules at actual operating conditions, and has advantages for integration of cells into modules. Lower current allows designing the module with a thinner window layer thereby reducing losses due to plasma absorption in the window layer. Decreasing the current density decreases the resistive power loss in the TCO. For the same design current, wider cells with fewer interconnects leads to higher active area by decreasing the relative inactive area of the module – the ratio of interconnect area to cell area. For the same module voltage, the temperature dependence of module voltage is lower for fewer higher voltage cells.

SSI's R&D Approach

From the industrial perspective, the full process sequence anticipated for use in large-scale production must be mastered and rigorously demonstrated. The SSI research approach is composed of two main elements:

- Experimentation and development using device structures that exercise all aspects of large area module production (17)
- Application of statistical process control (SPC) as the discipline to rigorously quantify process reproducibility, and application of statistical methods such as analysis of variation (ANOVA) to rigorously quantify experimental results (18, 19).

Prior to this subcontract, SSI abandoned development based on individual cells and defined a 10x10 cm twelve-cell monolithically interconnected "mini-module" baseline process. The structure of the mini-module is essentially a subsection of larger modules; therefore, fabrication of mini-modules demonstrates the full process sequence required for fabrication of larger modules. Process development using mini-modules allowed SSI to effectively address the most critical issues determining module yield at that time: 1) the uniformity and reproducibility of the absorber formation process, 2) the interaction of the substrate with the films, 3) performance losses near interconnects. Using mini-modules rather than large area modules allows processing and analysis of more parts and more process variations with a faster turn-around time.

Process predictability is a prerequisite for commercialization of thin-film PV since product performance ratings, yields and costs must be known before committing to produce products. Also, process predictability is essential for proper interpretation of process development efforts since experimental results may be ambiguous or misleading if compared to an unpredictable baseline process. SSI has

adopted SPC methodologies because SPC was developed to rigorously quantify process reproducibility and process capability; the essence of SPC is predictability (20). Equally significantly, SPC provides the measure of systematic progress as processes are developed and communication of this progress is typically best expressed in the language of the SPC discipline. For example, process characterization results are demonstrated to be "statistically significant" based on knowledge of process repeatability measured using the SPC discipline, and confidence in the appropriate interpretation of experimental results is gained through application of statistical methods such as ANOVA.

Subcontract Activities and Milestones

This subcontract work is divided into four Activities:

- Safety, Health and Environment.
- Device Structure and Design
- Process Development and Optimization
- Module Reliability and Packaging

The Safety, Health and Environmental activity encompass both in-house and team-oriented long-term research topics. Topics for this activity include definition of appropriate strategies for environmentally-conscious manufacturing, providing samples to testing labs to perform appropriate concentration and leach testing of completed modules and manufacturing scrap, evaluation of process options for non-Cd windows, evaluation of alternate selenium sources such as vapor phase elemental selenium and point-of-use generation of H_2Se, evaluation of no-lead solders and solderless lead attach/termination strategies, dry-reactant entrapment systems, and buffer deposition systems for improved utilization of the reagents to reduce waste.

The Device Structure and Design activity consist of primarily team-oriented and in-house long-term research topics targeting improved device performance, improved reliability, and definition of alternative buffer materials. Topics for this activity include collaborative efforts to model CIS devices, investigations of junction performance mechanisms, investigations of the role of Ga and S in CIS-based alloys, and investigations of alternative buffer materials and their effects on CIS-based devices.

The Process Development and Optimization activity encompasses in-house research to support the fabrication of module circuits. Topics for this activity include investigations of substrate preparation, investigations of sputtering processes, demonstration of large area uniformity, demonstration of control of the absorber film, studies of the reaction kinetics of the absorber formation process, development of process diagnostics, and interconnect formation process development.

The Module Reliability and Packaging activity addresses one of the remaining challenges for CIS technology. The origins of thermal transient behavior need to be identified and eliminated if possible. A package design needs to be developed which can enable completed modules to pass standard environmental qualification testing. Transient effects are important for many topics in addition to accelerated testing: process definition, measurement protocols, process predictability and understanding of device structures. For example, transient effects confound measurements made during module fabrication and final measurements to define product rating, and confound efforts to quantify the relative quality of alternative package designs. In many ways, the confounding of accelerated test results by transient effects delimit subcontract results for environmental studies. Therefore, the major discussion of transient effects, including topics that might alternatively be addressed in sections on Process Development or Device structure and Design, is in the Module Reliability and Packaging section.

Milestones for this subcontract are described in Table 1.

Table 1. Milestones.

Due Date	Champion Module ($0.4\ m^2$)	Representative Samples for IQT	One Kilowatt Module Sets
Beginning of Contract		10 [M1]	N/A
End of Phase I	13% [M2]	10 [M3]	10% @ min. $0.09\ m^2$ [M4]
End of Phase II		10 [M5]	11% @ min. $0.09\ m^2$ [M6]
End of Phase III		10 [M7]	12% @ min. $0.38\ m^2$ [M8]

The main headings in the body of this report correspond with the main tasks for this subcontract: Safety, Health and Environment, Device Structure and Design, Process Development and Optimization, and Module Reliability and Packaging. Highlights of accomplishments and advancements in CIS technology are presented for each task along with examples of subcontract activities.

An additional aspect of this subcontract is active participation in Thin Film Photovoltaic Partnership Program National CIS R&D Team. SSI has been involved with the "Absorber Team" and "Junction Team" and the Principal Investigator for this subcontract is the coordinator for the "Transient Effects Group." Although the results of several teaming activities will be discussed as they relate to SSI subcontract work, this report does not attempt to summarize the results for all of the extensive team activities.

Technical Review

Safety, Health, and Environment

SSI emphasizes a safe working environment and works with the photovoltaic community through the Thin Film Photovoltaic Partnership Program ES&H team to promote safety throughout the industry. Safety is an important ingredient of business success. The basic principle of safety is that all personal injuries are avoidable. Effective Safety programs requires constant attention and concentration for success. To this end, SSI has established internal safety and monitoring programs including:

- Safety Centers chartered to review the safety of SSI facilities on a monthly basis
- Monthly department meetings to review the findings of the safety centers and promote safety through presentation of safety related news and topical training
- An Equipment Safety Review Committee chartered to review safety considerations regarding the installation of new equipment, definition of experiments, or modification of existing equipment
- A General Emergency Response Team which trains for emergencies throughout SSI
- An Incident Review Committee to review actual or potential incidents and recommend improvements for safe operations
- Training programs on specific equipment and general safety related topics
- Monitoring of personnel for exposure to potentially hazardous materials

SSI is a member of the Thin Film Photovoltaic Partnership Program ES&H team, and accordingly, has participated in the following activities in conjunction with the TFPPP ES&H Team:

- Periodic team meetings
- Toxicology studies and environmental impact studies
- Exploration of technical approaches for removing and recycling module components

As a prerequisite to implementing a new large area reactor (discussed in a later section), SSI collaborated with the TFPPP ES&H group headed by Paul Moskowitz and supported by his associates at Brookhaven National Laboratories to avoid hazards resulting from system failure. These efforts included estimation of the potential fire or explosion hazards and definition of methods to avoid fire or explosion. The new large area reactor was implemented with a nitrogen reservoir to insure safety by limiting oxygen availability in the event of system failure.

Device Structure and Design

Device Structure and Design activities were pursued to:

- Improve module performance
- Improved process reproducibility and yield
- Gain understanding regarding the fundamental mechanisms responsible for transient effects and thereby eliminating or minimizing their impact
- Support module reliability and packaging development
- Support reactor scale up efforts.

The majority of these activities were pursued in support of other subcontract tasks and are discussed later in the pertinent sections of this report. During Phase 1 of this subcontract, the majority of device structure and design activities supported demonstration of reproducibility and yield for the baseline mini-module process. As discussed further in a later section (Baseline Process Development), the baseline process was repeatedly executed to rigorously demonstrate the reproducibility and yield of the process. Similarly, multiple Device Structure and Design activities, that are closely related to module packaging development and understanding of transient effects, are discussed in the later section titled "Module Reliability and Packaging." The remainder of this section will outline some of the efforts discussed in later sections and give examples of activities that can be uniquely characterized as Device Structure and Design activities.

To define terms for this section, the nomenclature used by SSI for three types of absorber formation reactors will be addressed before addressing the main distinctions between these reactors in later sections of this report. SSI demonstrated the need to abandon the large area reactor, the "Phase 1 large area reactor," used prior to and into Phase 2 of this subcontract. A smaller reactor referred to as the "baseline reactor" was essentially unchanged throughout this subcontract. SSI built a new large area reactor, the "Phase 2 large area reactor," which is a more direct scale-up of the smaller baseline reactor.

The following process scale up efforts were supported by Device Structure and Design activities:

- Scaling of the CdS deposition process
- Incrementally improving substrate preparation techniques
- Exploring process condition variations to demonstrate their impact on absorber properties
- Mimicking proposed and observed Phase 1 large reactor conditions in the baseline reactor with emphasis on understanding the transfer of the baseline process to large area reactors
- Similarly, mimicking proposed and observed Phase 2 large reactor conditions in the baseline reactor with emphasis on understanding the transfer of the baseline process to large area reactors

For example, the culmination of surface preparation studies that were motivated by scale up activities resulted in the definition of an in-house surface preparation process equivalent to or slightly better than the previous baseline process. Data in Figure 6 indicates that the new baseline process yields an approximately 3-point improvement in efficiency over the previous baseline process.

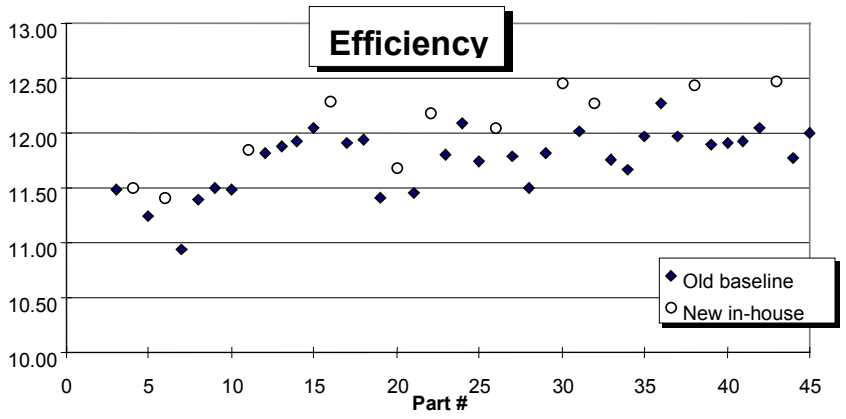


Figure 6. Comparison of new in-house and earlier surface preparation process.

Absorber formation runs designed to simulate the Phase 2 large area reactor process using the baseline reactor were pursued to gain a better understanding of the impact of reaction process parameters on adhesion. Poor adhesion was a problem for initial runs using the Phase 2 large area reactor. Nearly 50% of the parts from these runs were rejected after ZnO deposition due to peeling, and tape pull tests also indicated poor adhesion. Further experiments varying the selenium and sulfur introduction sections of the absorber formation process were performed in the baseline reactor to determine which section of the large area reaction process is responsible for poor adhesion. Result are summarized in Table 2 where an adhesion scale from 1 to 10 is used with 1 denoting poor adhesion and 10 denoting adhesion of the baseline process. Spontaneous adhesion failure after ZnO occurred only for simulation of both the selenium and sulfur introduction sections of the large area reactor process. Intermediate adhesion was obtained for the combinations of the baseline and large area reactor selenium and sulfur introduction sections of the process.

Table 2. Dependence of relative adhesion on absorber formation process.

Absorber formation process section		Relative Adhesion
Selenium introduction	**Sulfur introduction**	
Large area	Large area	1
Large area	Baseline	3
Baseline	Large area	4
Baseline	Baseline	10

Both the selenium and sulfur introduction sections of the initial large area reactor process have a similar detrimental impact on adhesion with the selenium introduction sections of the process having a somewhat greater impact. The results of these studies were combined with reactant concentration modeling to define processes for improved absorber adhesion in the Phase 2 reactor.

Adhesion and electrical performance were dependent on location in the reactor for all of the above variations in selenium and sulfur introduction. This interaction between part location and orientation was also the subject of investigation using both the large area and baseline reactors. Statistical analysis of the SSI baseline process indicated lower performance for absorbers formed at one position in the baseline absorber formation reactor. The first occurrence of lower performance for this position correlated with implementation of a change in substrate preparation. These devices exhibited a Voc that was systematically 5 points lower than for all other devices from the same absorber formation lot. Inductively coupled plasma mass spectroscopy (ICP) analysis indicated that the ratio of sulfur to selenium in the absorber is dependent on location in the reactor. These results furthered understanding of the importance of materials of construction and physical layout in reactor design. In turn, the understanding gained was applied to define a change in reactor layout with the result of decreasing the electrical performance dependence on location.

Additional insights achieved by comparing changes in the baseline reactor process with the large area process are discussed in the following sections titled “Baseline Process” and “Process Scale-up.”

Absorber structure improvements were pursued with emphasis on improvements in module performance. Efficiency gains are feasible by adjusting the relative amounts of the constituent elements or elemental profiles – grading – in the absorber. Voltages somewhat above baseline values were achieved with minimal improvement in efficiency by changing reaction conditions to increasing the total sulfur content in the absorber and alter the grading of the sulfur.

Increases in the gallium content also increased the open circuit voltage; however, with no improvement in efficiency for the process conditions explored. In addition to baseline precursors, the experimental matrix included Gallium deposited on baseline precursors at the Institute of Energy Conversion (IEC) and Showa Shell Seikyu, K.K. Standard conditions were used to react the precursors to form graded absorbers. Device parameters are plotted in Figure 7 as a function of the bandgap derived from spectral response measurements (this bandgap measurement is discussed further in "Process Scale Up"). Measured bandgap increases with increasing gallium content. Improvements in open circuit voltage are observed with the accompanying counter variation in short circuit current. However, efficiency is not improved. Open circuit voltage correlates with gallium content near the front of the absorber as determined by SIMS analysis from NREL. Voltage nonuniformities were observed which are believed to be related to nonuniformity of gallium deposition. Defects in the absorber film, which are not observed for the baseline process, were observed in SEM (IEC) and optical micrographs . These observable nonuniformities and defects are assumed responsible for lower fill factor and lower efficiency for higher gallium concentrations.

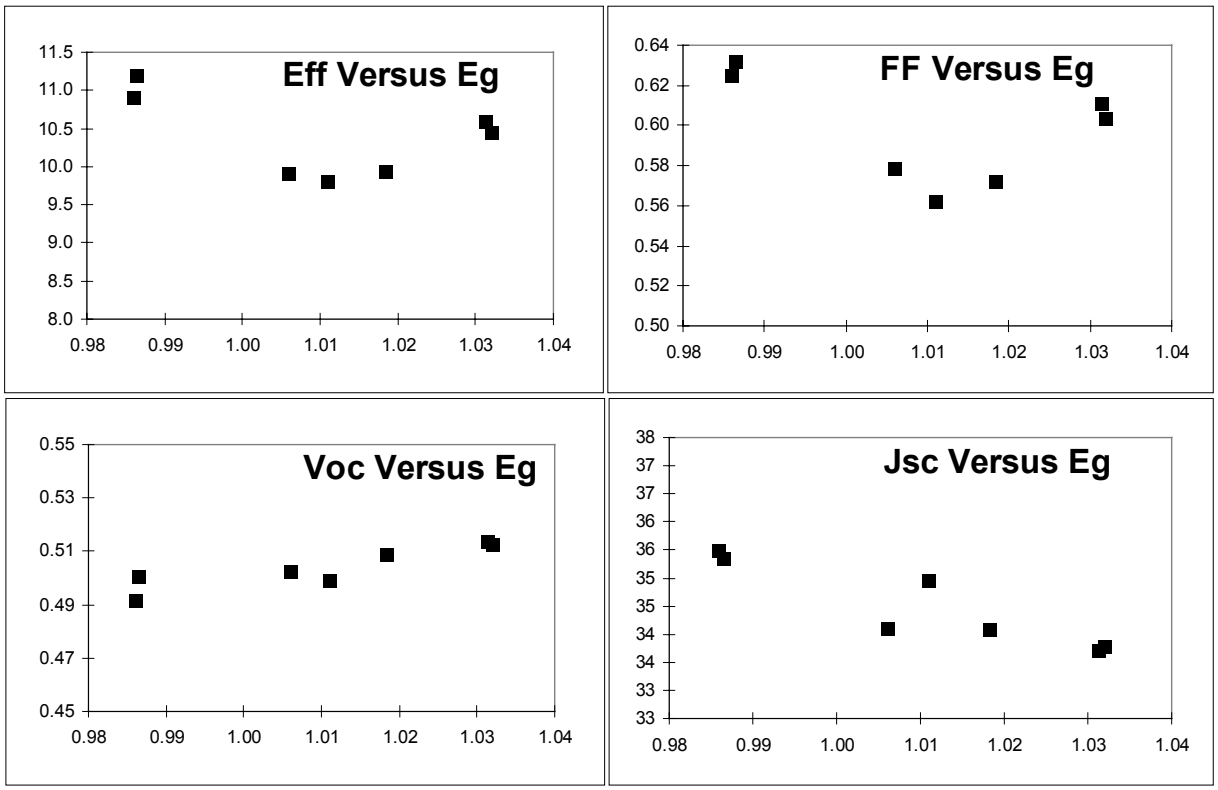


Figure 7. Device parameters as a function of bandgap for absorber structure with varied gallium content (abscissa – Bandgap in units of eV) .

Device performance for an alternative method of sulfur introduction was also explored. Figure 8 depicts the changes in open circuit voltage and short circuit current as a function of the ratio of sulfur to selenium in the absorber as determined by ICP analysis. Open circuit voltage increases were achieved at the expense of lower short circuit current with minimal effect on efficiency except for the highest sulfur contents that exhibited lower fill factors.

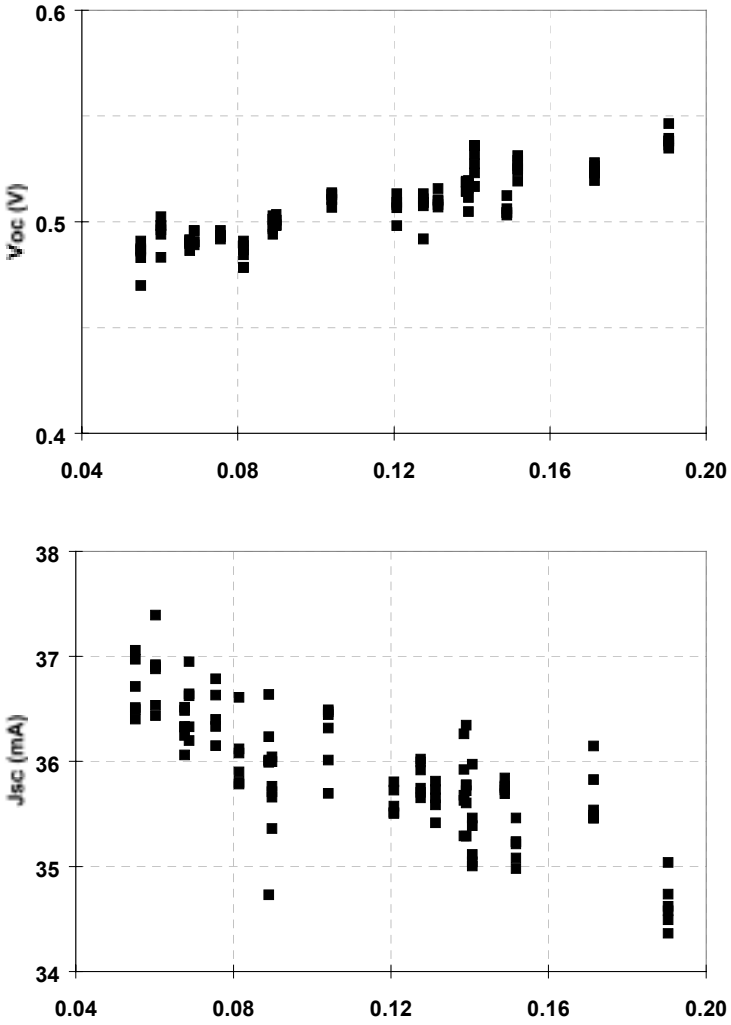


Figure 8. Open circuit voltage and short circuit current as a function of the ratio of sulfur to selenium (abscissas – relative concentration).

Process Development and Optimization

Baseline Process Development

During Phase 1 of this subcontract, the baseline process was repeatedly executed to demonstrate the potential of the technology and in support of scale up efforts. Demonstration of a predictable baseline was essential to allow comparison of large area and baseline results with confidence that effects of a particular process change could be distinguished from special causes. As seen in Figure 9, a reproducible low variation 10x10 cm mini-module baseline was demonstrated for over two thousand mini-modules.

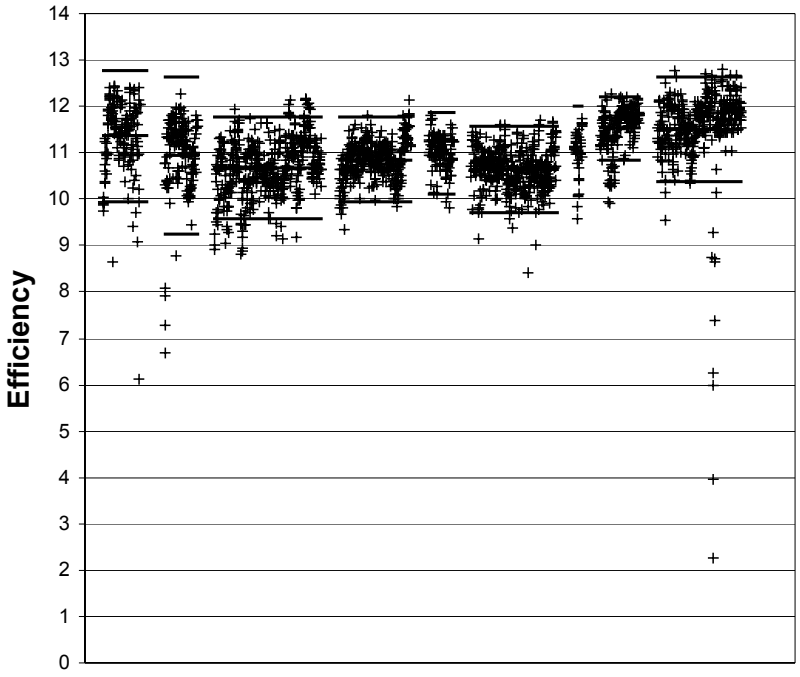


Figure 9. Control chart-showing efficiency of more than two thousand mini-modules (abscissa – module identifier).

Figure 9 presents data in one of the typical formats for the SPC methodology. The SPC methodology provides a foundation for judging process reproducibility that is represented graphically by charting processing results including the process average, "upper control limits," and "lower control limits." Averages and the upper and lower control limits over timeframes when the process conditions were held constant are represented as horizontal lines in the figure. Results which fall within these control limits are essentially equivalent, differing only because of the random or "common cause" variation inherent in any stable, controlled process. Results that fall outside these limits can only be explained by "special causes" which reveal errors in executing the baseline process. This data presentation format emphasizes and focuses attention on eliminating the special causes of process instability, and then, on continually reducing the sources of common-cause variation inherent in the stabilized process.

During the first phase of this subcontract, laminated baseline mini-module efficiencies after outdoor exposure typical of in-service conditions averaged 12.4% (Figure 10).

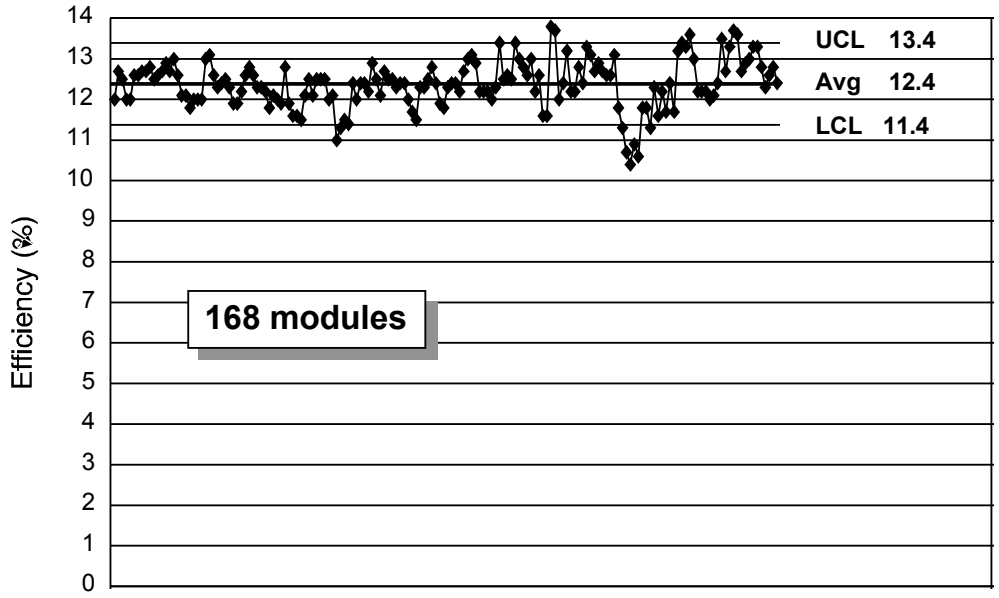
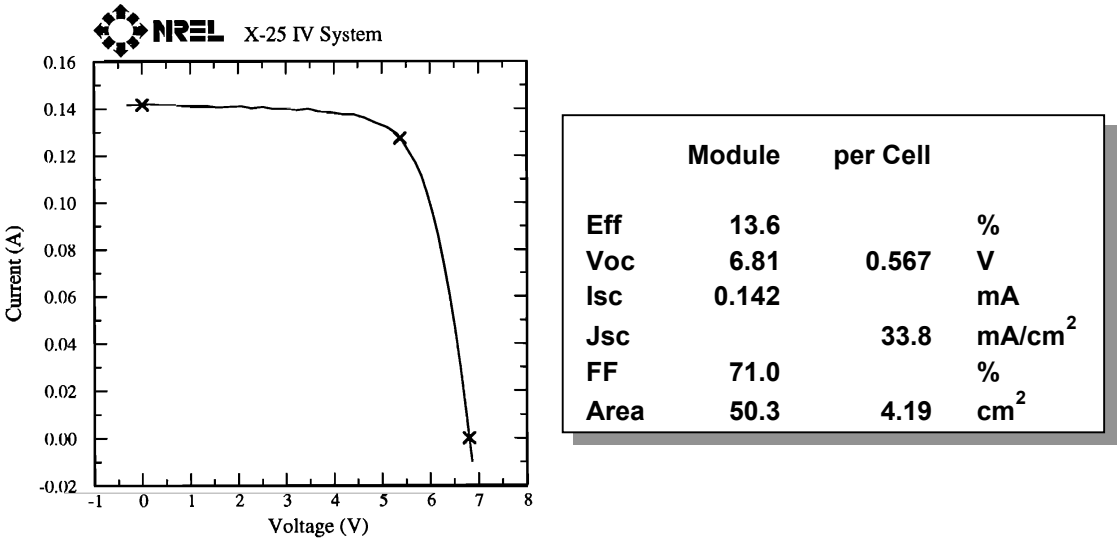


Figure 10. Control chart showing laminated mini-modules averaging 12.4% efficiency after a minimum of two weeks of outdoor exposure (abscissa – module identifier).

NREL measured a champion efficiency for a mini-module in this data set. The current versus voltage curve and device parameters measured by NREL for a 13.6% aperture area efficient mini-module is displayed in Figure 11.



	Module	per Cell	
Eff	13.6		%
Voc	6.81	0.567	V
Isc	0.142		mA
Jsc		33.8	mA/cm^2
FF	71.0		%
Area	50.3	4.19	cm^2

Figure 11. 13.6% aperture area efficiency mini-module as measured by NREL

Module and average cell parameters are listed in Table 3 for four laminated mini-modules with efficiencies averaging 13.9% that were delivered to NREL as M2 deliverables.

Table 3. Laminated mini-modules averaging 13.9% efficient as M2 deliverables (SSI measurements).

ID #	Eff	Module Voc (V)	Cell Voc (V)	Module Isc (mA)	Cell Jsc (ma/cm^2)	FF	Area cm^2
216-62	13.8	6.77	564	0.148	34.9	0.701	50.9
216-38	13.8	6.79	566	0.143	34.3	0.708	50.0
214-32	13.8	6.89	574	0.144	33.9	0.708	51.1
214-30	14.1	6.91	576	0.144	34.6	0.711	49.9

As discussed in the following section titled "Process scale-up," a large area reactor was not available while SSI designed and built a new large area reactor. Therefore, during the second phase of this subcontract, the baseline reactor was used to produce subcontract deliverables and introductory CIS-based products. Instead of the standard 10x10 cm circuit plate, fixtures for the baseline reactor were procured to process 10x30 cm circuit plates. Simultaneously, baseline 10x10 cm circuit plate fabrication continued through the end of the subcontract to demonstrate a reproducible low variation process, and in support of experimentation and process scale-up efforts.

Electrical performance identical to baseline 10x10 cm circuit plates was achieved for 10x30 cm circuit plates after addressing adhesion issues. A correlation between the number of parts in the absorber formation process and adhesion between the CIS and Mo was observed. Poorer adhesion for the area between the pattern in the Mo (P1) and the pattern in the CIS (P2) was also observed and correlated with changes in the substrate preparation and Mo deposition process implemented in conjunction with fabrication of deliverables. Modification of the substrate preparation and Mo deposition process allowed high throughput, good Mo patterning quality over large areas, and improved near-P1 adhesion. Although significant improvements were demonstrated, sporadically poor adhesion near the Mo pattern, and substrate to substrate variations in laser scribe quality, continued to be observed.

As discussed further in the following section titled "Module Reliability and Packaging," these 10x30 cm circuit plates fabricated using the baseline reactor were combined to form prototype ~30x120 cm modules, and 5 and 10 W products. SSI delivered a 1 kW set of modules (Figure 12) and an additional 10 modules for testing to NREL, fulfilling the M3 and M4 subcontract deliverables. The 1 kW set of modules replaced an existing 1 kW array based on an older absorber formation technology. Performance improvements for this array are discussed in the following section.

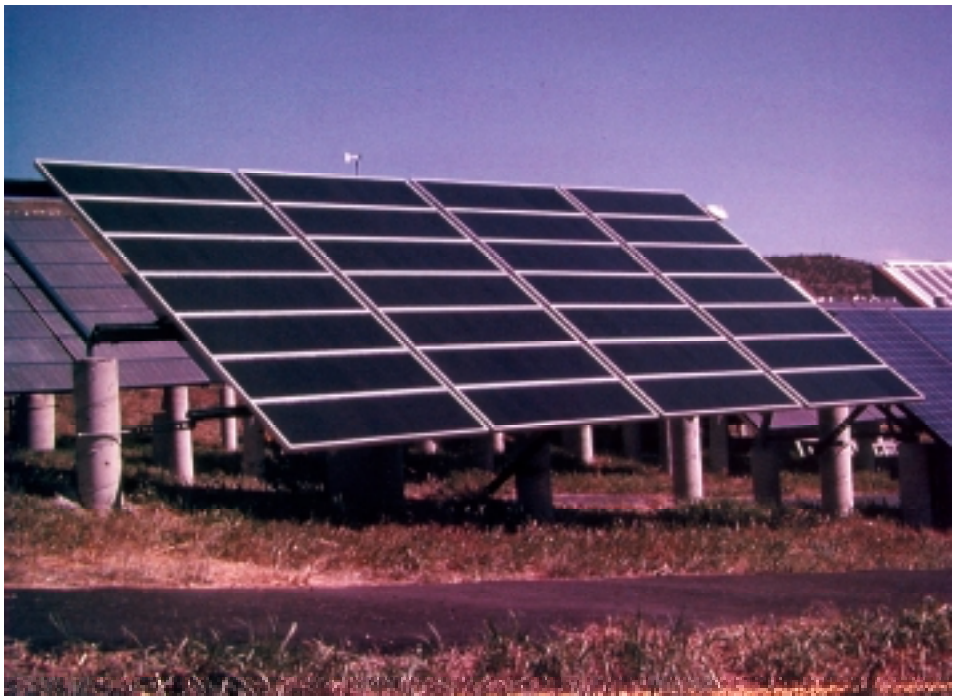
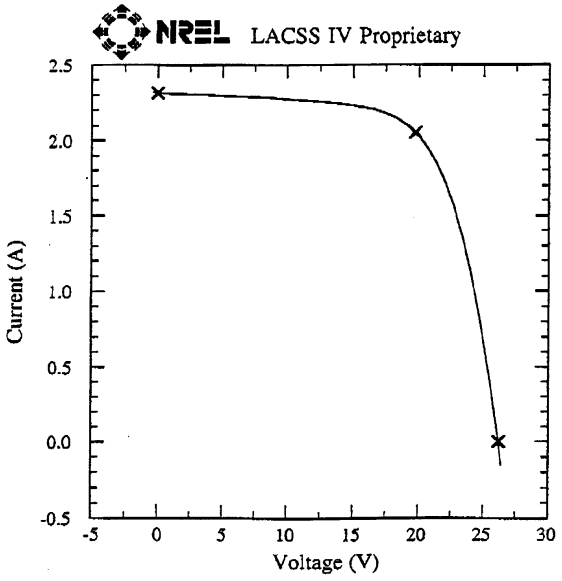


Figure 12. One kilowatt array - graded sulfur absorbers (1997).

A module identical to the modules of this array but with an aperture physically masked to exclude both bus ribbons was confirmed by NREL to produce 40.6 watts for a confirmed world-record efficiency (1997) of 11.1 percent on 3665 cm2 (Figure 13). This demonstrated efficiency exceeds the 1995 DOE efficiency goal for CIS prototype modules.



	Module	per Cell	
Eff	11.1		%
Voc	26.2	0.524	V
Isc	2.3		A
Jsc		31.6	mA/cm^2
FF	66.9		%
Area	3665	73.3	cm^2

Figure 13. Record efficiency (1997) of 11.1 percent on an aperture area of 3665 cm2

SSI also introduced two new CIS-based products. The product designations are ST5 and ST10 which are 21x33 cm, 5 watt and 39x33 cm, 10 watt modules designed for use in 12 V systems (Figure 14). The aluminum framed modules are fabricated from two or more circuit plates processed in the baseline reactor. SSI delivered product samples to NREL as M5 and M6 contract deliverables and NREL reported 9.6% aperture area efficiency (11.2 % circuit plate aperture area) which at that time (1997) was the highest efficiency of any commercial non-crystalline module.

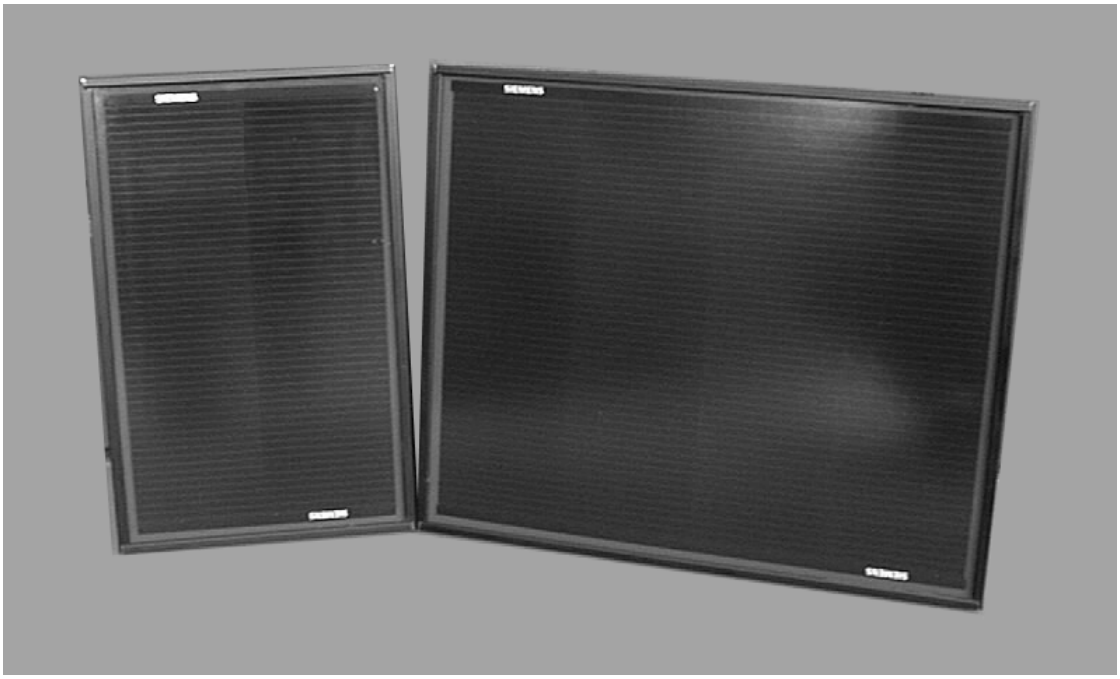


Figure 14. Introductory CIS-based 5 and 10 W products.

Process Scale-up

Process scale-up proceeded from the foundation of the reproducible low variation baseline process. Transfer of the mini-module process first to a 30x30 cm part size in the Phase 1 large area reactor included the tasks of calibration and transfer of baseline process to larger reactor, evaluation of the large reactor process, and evaluation of uniformity. Characterization of the large area process and process development to isolate the sources of performance differences between the baseline process and the large area process were greatly aided by comparison with a stable and therefore predictable baseline process. For each step in the process, the impact of the larger part size was tested in the baseline. For example, by cutting the 30x30 parts into nine 10x10 parts, the uniformity of the performance of the larger part was measured using the baseline process. Such experiments indicate that the larger-area parts should be able to achieve the same level of performance as the smaller parts.

However, during Phase 1 of the subcontract, the performance of large-area circuits did not reached the same level as the performance of the 10x10 mini-module baseline. The difference between the baseline and large area processes was isolated to the formation of the absorber in the larger reactor.

Baseline and 30x30 cm efficiency results are plotted in Figure 15. The performance of the larger parts is inferior to baseline performance; baseline circuit plate efficiencies are about 11.5% whereas 30x30 cm performance is about 8%. However, the same performance for 10x10 and 30x30 cm circuits plates was obtained when the absorbers for both substrate sizes were formed in the Phase 1 large area reactor (Figure 16). This indicates that the part size itself is not the cause of the observed performance differences.

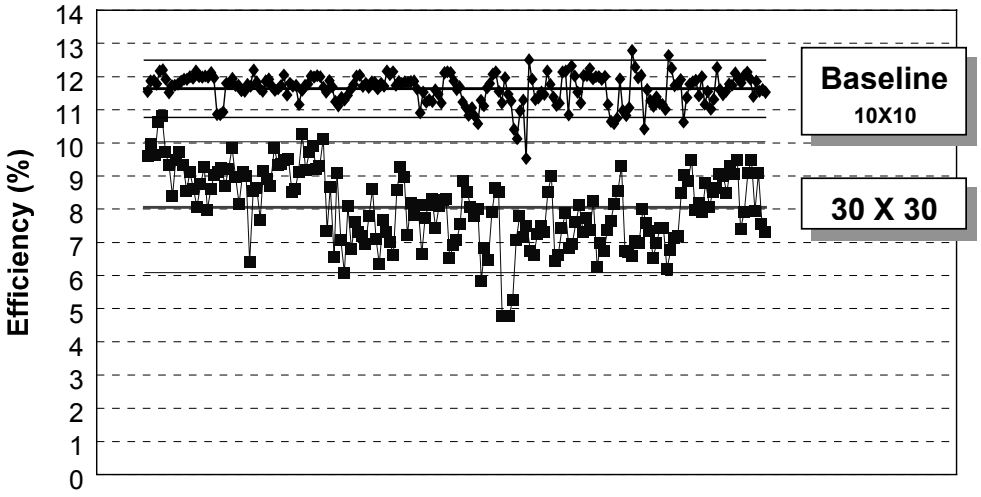


Figure 15. Comparison of the 10x10 baseline and 30x30 circuits processed in the Phase 1 large area reactor (abscissa – module identifier).

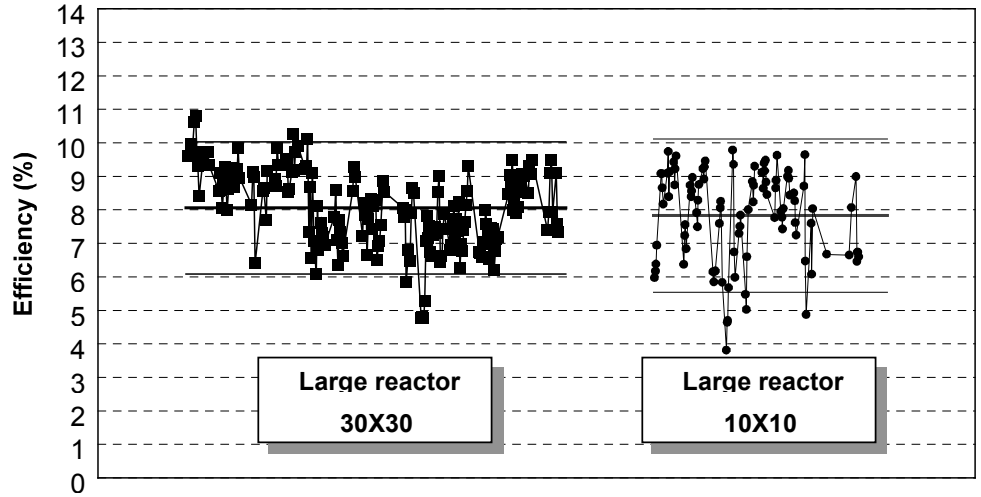


Figure 16. Comparison of 10x10 and 30x30 circuits processed in the Phase 1 large area reactor (abscissa – module identifier).

The absorbers obtained from the baseline process and the large reactor were compared using bandgap measurements and SIMS. Bandgap determined from spectral response measurements indicates a difference in the absorber structures for absorbers from the baseline and large area reactors. Figure 17 is a plot of the square of quantum efficiency versus photon energy for multiple devices from both the baseline and large area reactors. The intercept on the energy axis is taken as a measure of optical bandgap which is actually a convolution of the affects on absorption and collection through the varying bandgap structure of these absorbers [P1, 4, 6]. Differences in this measure of bandgap, ~0.99 eV for baseline and ~1.02 eV for absorbers from the large reactor, imply a difference in the structure of the absorbers.

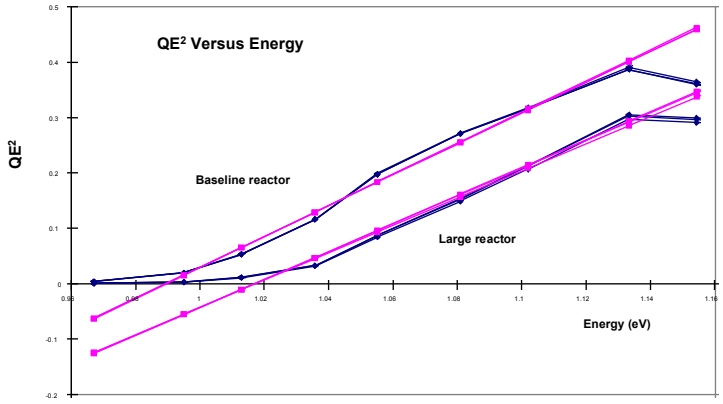


Figure 17. Comparison of bandgaps for absorbers from different reactors.

SIMS analysis of baseline absorbers and absorbers from the Phase 1 large area reactor identify the differences in absorber structure. The profile of sulfur concentration is the primary difference between absorbers from the two reactors (Figure 18). The concentration of sulfur is highest at the front of the

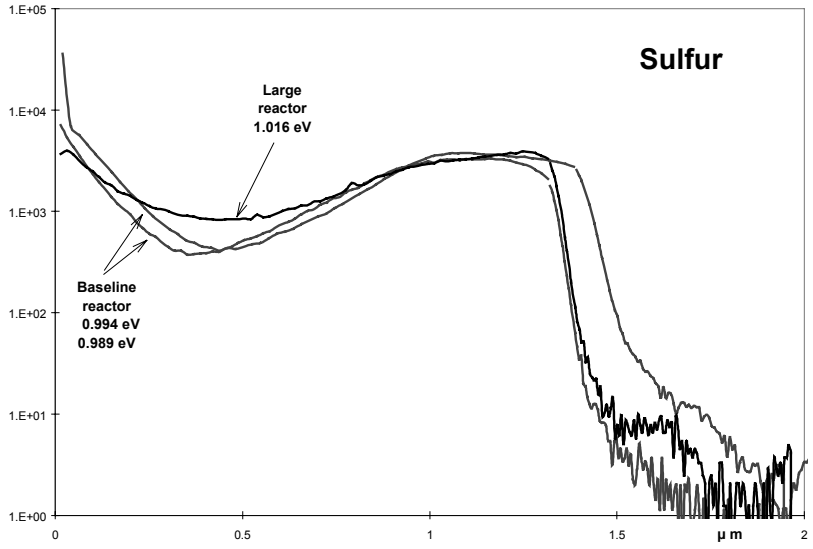


Figure 18. Comparison of SIMS sulfur profiles for absorbers from different reactors.

absorber and decreases toward the center of the absorber for both reactors. The sulfur profile for baseline absorbers is "sharper"; the sulfur profiles have a higher gradient from the front to the center of the absorber. The concentration of sulfur at the front is higher and the concentration near the middle of the absorber is lower for baseline absorbers.

Further analysis of absorber structures and device performance for absorbers and circuit plates from the baseline and Phase 1 large reactor identified additional differences. The following summarizes the observed differences:

- Bandgap of the absorber
- Elemental concentrations in the absorber
- Elemental concentrations profile in the absorber
- Contact resistance
- Relative adhesion above the interconnect scribe in the molybdenum
- Visual appearance of the molybdenum after scraping off the absorber
- The relative amount of sulfur and selenium in the molybdenum

These observed differences between circuit plates from the two reactors were related to the design of the large reactor through variations in process condition to demonstrate their impact on absorber properties and by mimicking large reactor conditions in the baseline reactor.

During Phase 2 of this subcontract, studies of the differences between reactors continued. For example, ICP (and other) analysis of samples from the two reactors indicated that process conditions for the large area reactor were more similar to the baseline reactor after cleaning. Subsequent operation of the large area reactor led to further divergence from the process conditions for the baseline reactor. In support of these findings, quantum efficiency based bandgap measurements (Figure 19) indicated increasing bandgap for successive reaction runs after cleaning the large area reactor.

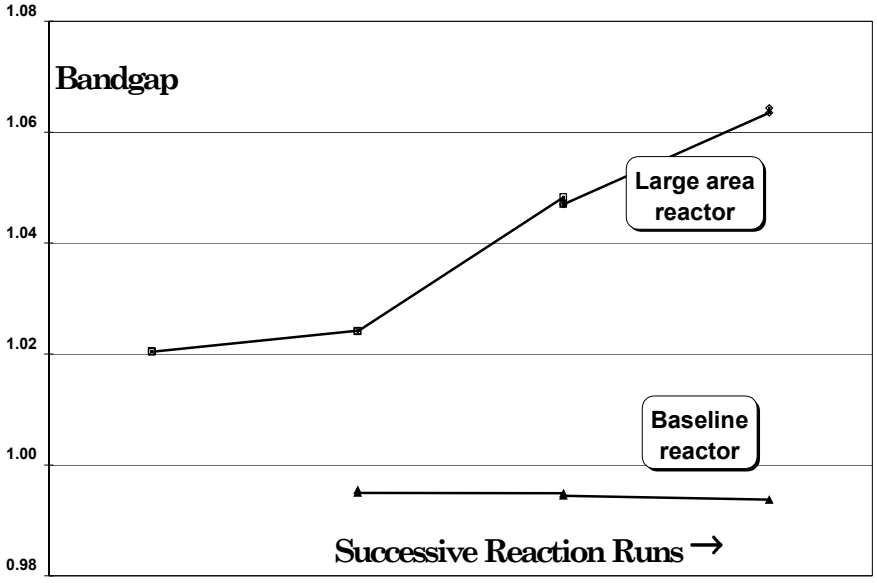


Figure 19. Bandgap for successive runs in the baseline and large area reactors.

Whereas this bandgap versus reaction run trend for the large reactor is distinct, device parameter versus bandgap trends were relatively week and performance in the large area reactor remained inferior. Also, cleaning the large area reactor decreased interconnect contact resistance to values similar to values for the baseline process. In summary, these studies and refinements of process condition allowed adjustment of most but not all of the process conditions in the large area reactor to more closely mimic process conditions in the baseline reactor. This mitigated most but not all of the observed differences between the process achieved in the two reactors. Similarly, these studies allowed isolation of the remaining differences between reactors to differences in the materials of construction and the physical design of the large reactor.

In response to these findings, SSI designed and build a new large area reactor – the Phase 2 reactor. Safe use of potentially hazardous reactants was the first consideration. SSI, with help from the TFPPP ES&H group headed by Paul Moskowitz and supported by his associates at Brookhaven National Laboratories, defined a reactor to avoid potential fire or explosion hazards resulting from system failure. These efforts progressed through the following subtasks:

- Determining the potential hazard based on the energy released and the timeframe for release
- Reviewing hazard avoidance methods
- Implementing the best hazard avoidance method

Four main uncertainties hampered determining the energy released and the timeframe for release:

- Adequate thermodynamic data was not available for H_2Se.
- The appropriate final states for the products of potential reactions was uncertain.
- The reactions that would occur for actual conditions were unknown. For the example of H_2Se, an oxygen deficient reaction is a reasonable scenario that could lead to oxidation of just hydrogen rather than oxidation of both the hydrogen and selenium.
- The dynamics of the reactions, mixing of air and fuel, etc. were unknown and expected to be dependent on system geometry and the specifics of a failure.

Brookhaven National Laboratories performed worst case calculations indicating potential damage to SSI infrastructure based on SSI supplied data on gas concentrations, thermodynamics, system geometry, and infrastructure. SSI considered fuel limiting and oxygen limiting control measures. Energy absorbing control measures were considered inappropriate. SSI implemented a nitrogen blanket and reservoir with an oxygen sensor to insure safety based on limiting oxygen availability in the event of system failure.

Based on the advances in understanding regarding the influence of reactor design on performance, SSI designed and built a new large area reactor that is a more direct scale-up of the baseline reactor. This reactor became operational late in Phase 2 of this subcontract. Success with this reactor was initially demonstrated by circuit performance for 28x30-cm circuits averaging 10.6% that compared very favorably to the 10x10-cm baseline. The rest of this section primarily discusses continued success with this reactor.

Prior to and early during Phase 3, circuit plates smaller than ~30x120 cm were typically processed in the Phase 2 large area reactor. The few ~30x120 cm circuit plates that were processed in the Phase 2 reactor were then cut to smaller circuit plates before further processing. This was done for compatibility with interim process definitions and infrastructure used to produce subcontract deliverables and introductory CIS-based products. Beginning early during Phase 3, all processes were scaled to a ~30x120 cm plate size; only ~30x120 cm circuit plates were processed in the Phase 2 large area reactor and through all subsequent device formation processes. These ~30x120 cm circuit plates were then laminated as

~30x120 cm modules or cut to smaller sizes after all device fabrication processes. Fabrication of ST5 and ST10 products from 10x30 cm circuit plates produced in the baseline reactor was discontinued.

About 1300 ~30x120 cm circuit plates were produced between January and November of 1998 including 18% that were dedicated to experiments (Figure 20). The process exhibits generally good control for extended periods with an average efficiency of 10.8%. Periodic shifts in the short-term average efficiency between about 10.25 and 11.25 are driven by shits in Voc and FF and appear to result from batch-to-batch variability in precursor or base electrode preparation. Similarly, periodic shunting along the laser scribed pattern lines in the Mo base electrode appears to result from batch-to-batch variability in base electrode preparation. Mechanical yield, the fraction of all substrates introduced into production which pass intermediate inspections before IV testing, was 74%. Electrical yield depends upon the choice of lower specification limit; 85% yield at 10% minimum circuit efficiency and 96% yield at 9% minimum efficiency.

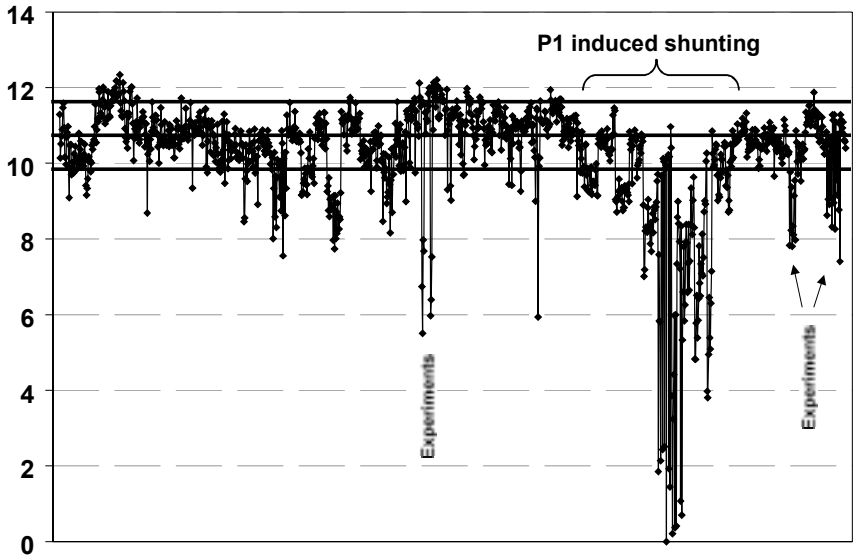
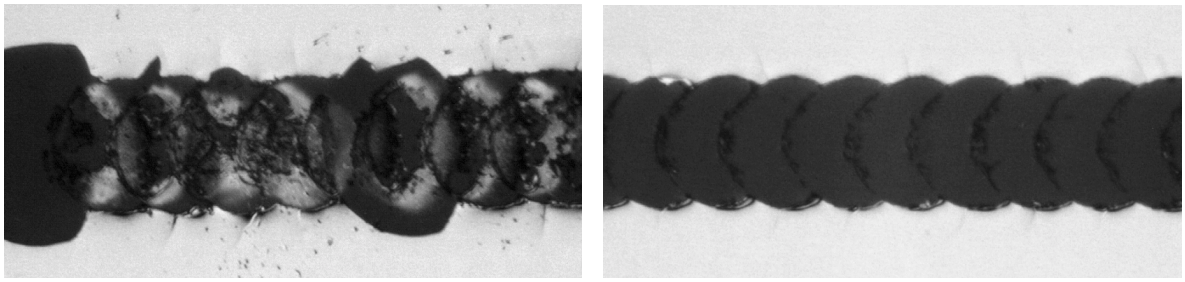


Figure 20. CIS Circuits Produced January through November 1998 (abscissa – module identifier).

Shunting along the laser pattern 1 (P1) scribes sporadically caused poor performance. Although shunting along the P1 scribes is not always correlated with the appearance of the P1 scribes, shunting along P1 scribes may be due to cracks in the Mo adjacent to the P1 scribes or due to adhesion failure at the Mo/glass interface immediately adjacent to the P1 scribes. For constant laser patterning conditions, shunting along the P1 scribes correlated with the base electrode deposition batch but did not correlate with the substrate preparation batch.

Experiments varying electrode deposition conditions demonstrated that the appearance of P1 scribes, and the degree of variation of this appearance from the edge to the center of a substrate, are dependent on Mo deposition conditions. Variation in P1 scribe appearance from the edge to the center of a substrate (Figure 21) can be extreme for improper Mo deposition conditions and may even result in inadequate isolation between adjacent cells.



Edge Center

Figure 21. Substrate edge to the substrate center variation in P1 scribe appearance.

While the impact of periodic shifts in the short-term process average for ~30x120 cm circuit plates is relatively small, this variation was explored through additional monitoring of the laser process and by continued tracking of batch to batch process dependence. Average electrical performance for ~30x120 cm circuit plates continued to vary throughout this timeframe primarily due to changes in Voc although mechanical and electrical yields were high (92% and 97% respectively) as judged by the specifications for ST5 and ST10 products. Although an understanding of the relationships between Mo electrode deposition conditions and P1 scribe appearance was gained through these experiments, the batch-to-batch variability in P1 scribe appearance and the batch-to-batch variability in shunting along P1 scribes are not yet well understood.

Multiple generations of interconnect test structures have been developed at SSI to evaluate interconnect performance independent of solar cell device measurements. Interconnect test structures have been developed to characterize the quality of the pattern in the Mo (P1), resistance of the interconnect between adjacent cells (P2), and measurement of ZnO sheet resistance. P2 interconnect test structures are module plates with double back-to-back interconnects along the current path of the module as illustrated in Figure 22. The resistance of multiple interconnects can be measured as a survey of the interconnect

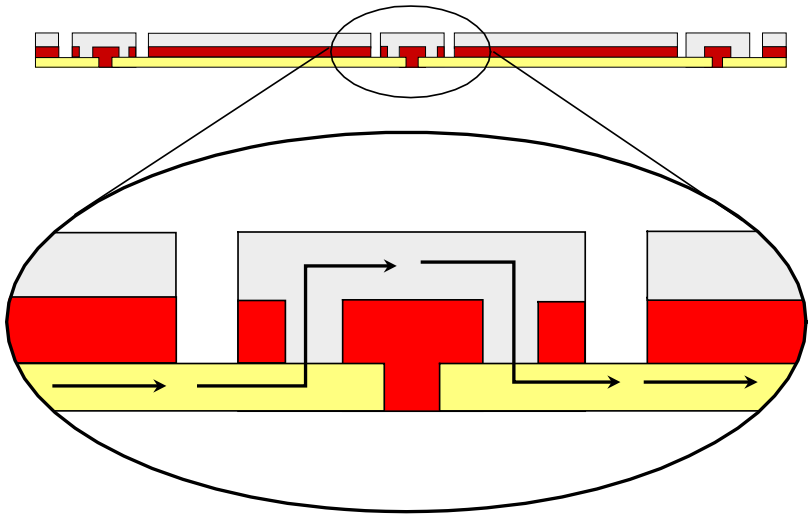


Figure 22. One type of interconnect test structure.

performance for a full module, or measurements across adjacent Mo pads can be made as a diagnostic for individual interconnects. Variants of this structure have been defined to evaluate various aspects of device structures. Both interconnect contact resistance and ZnO sheet resistance can be measured by varying the separation of the double back-to-back interconnects. The structure can also be laminated and subjected to environmental testing to evaluate the durability of various interconnects structures and interconnect materials.

Another type of test structure and methodology was developed to characterize the quality of the pattern in the Mo by comparing the voltage of devices with and without extra scribes down the length of the devices. Equivalent voltage with and without this extra scribe indicates that patterning of the Mo does not influence device performance. This, and previously discussed P1 test structure approaches, have the disadvantage that they require processing of a special device structure, and measurements at Voc only identify gross shunting.

A new approach was developed during this subcontract in conjunction with exploring the possibility that poor adhesion along P1 leads to shunts and therefore degrades module performance. Instead of processing a special P1 test structure, normal modules can be subjected to further diagnostics that yield better information than the P1 test structure. The versatility of this approach allows application to systematic experiments involving dedicated groups of circuit plates, or application as a diagnostic for low performance circuit plates on an as needed basis. As a diagnostic, ~30x120 cm modules are typically first cut into strips to address variation across the ~30x120 cm plate. The best and worst strips are voltage mapped, and then remapped after an additional scribe is made in the ZnO to isolate each cell from the adjacent pattern in the Mo. Lower voltage before the additional scribe is an indication of shunting in the region adjacent to the pattern in the Mo. Voltage mapping at about 20% of one sun was established as a standard based on studies of the sensitivity of this methodology to intensity.

This approach has been applied to explore the cause of periodic shifts in the short-term process average by voltage mapping circuit plates from module groups with normal and lower than normal fill factors. Large area ~30x120 cm circuit plates with normal and lower than normal performance were diced into 14 strips. In Figure 23, results of voltage mapping of 4 of the 14 strips are plotted before (ϖ) and after (♦) making additional scribes adjacent to the pattern in the Mo. Lower Voc prior to making additional scribes, and significant improvement after scribing, are observed for some strips from ~30x120 cm circuit plate with both typical and lower performance. Therefore, periodic shifts in FF do not correlate with shunting in the region adjacent to the pattern in the Mo.

Correlation between lower Voc and FF, and the precursor or base electrode batch has been observed. Also, periodic shunting along the laser scribed pattern lines in the Mo base electrode has been correlated with batch-to-batch variability in base electrode preparation. Therefore, shunting in the vicinity of the pattern in the Mo may degrade the performance of individual ~30x120 cm circuit plates and the frequency of this degradation may be dependent on batch-to-batch variability in base electrode preparation; however, periodic shunting along the laser scribed pattern lines in the Mo base electrode is not solely responsible for the periodic shifts in the short-term process average.

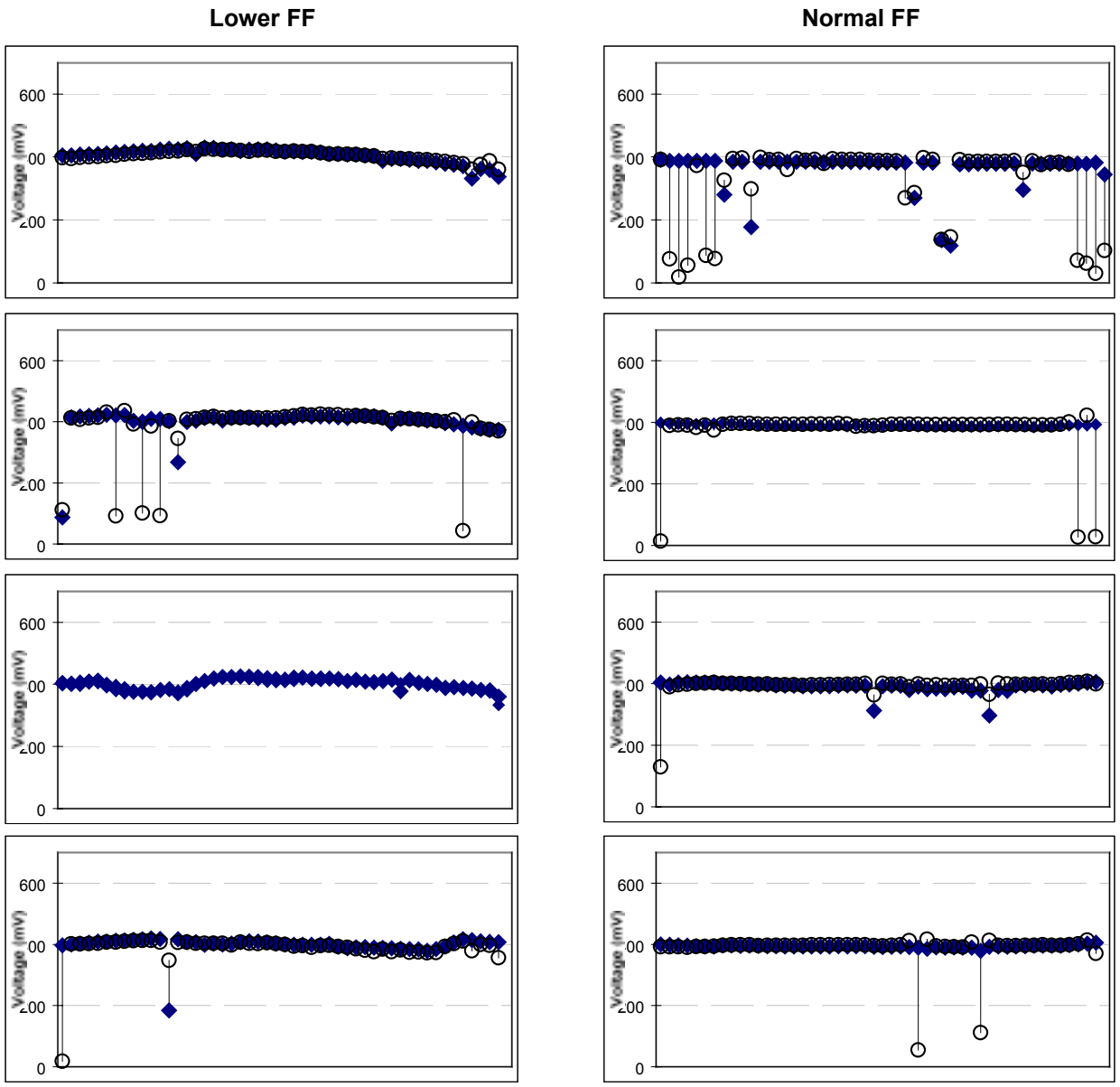


Figure 23. Voltage mapping - voltage at 0.2 suns versus module cell # for modules with normal and lower FF - before (O) and after (♦) making scribes adjacent to the pattern in the Mo (abscissa - individual cells within a module).

Other methods to determine the source of process variability were also explored. For example, bandgap (determined from the intercept on the energy axis of a plot of the square of quantum efficiency versus photon energy) has also been used to explore the reasons for variation in the average electrical performance for ~30x120 cm circuit plates. The intercept on the energy axis is taken as a measure of optical bandgap. Bandgap measurements were made for devices representing the best and worst performance from groups of ~30x120 cm circuit plates with generally high and low performance (Figure 24). There is no correlation between bandgap and performance for devices representing the best and worst performance or for groups with generally high or low performance.

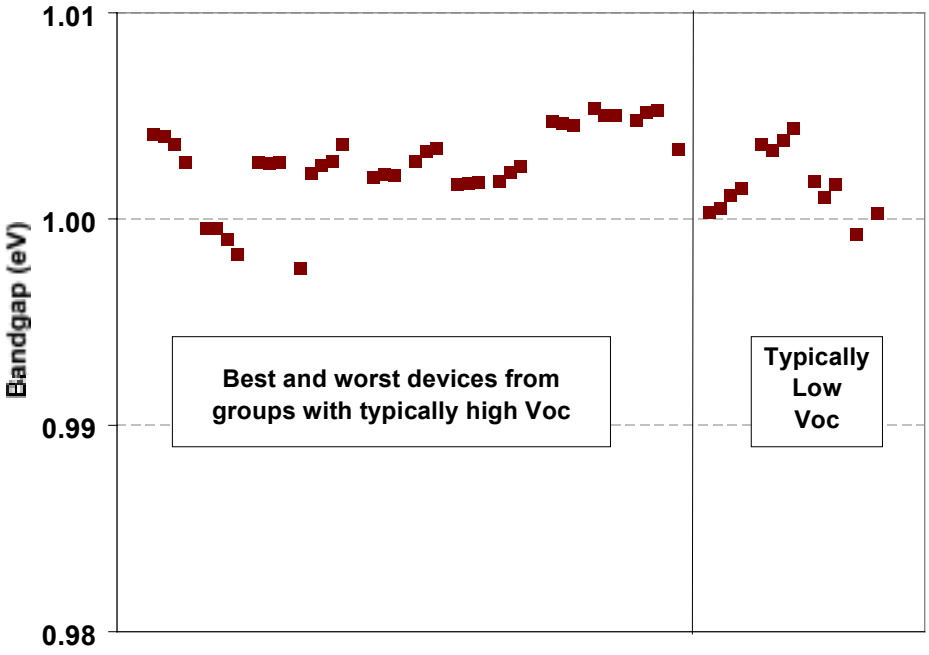


Figure 24. Bandgap measurement results as an example of other explorations of the source of process variability (abscissa – module identifier).

An alternative P1 process was pursued to eliminate the potential problems associated with cracks in the Mo adjacent to the laser P1 scribes or adhesion failure at the Mo/glass interface immediately adjacent to the laser P1 scribes. Jet etching (U.S. Patent 4599154, Electrically Enhanced Liquid Jet Processing) is the use of liquid jets to scribe lines in the Mo electrode by electrically enhanced etching. Narrow jets of

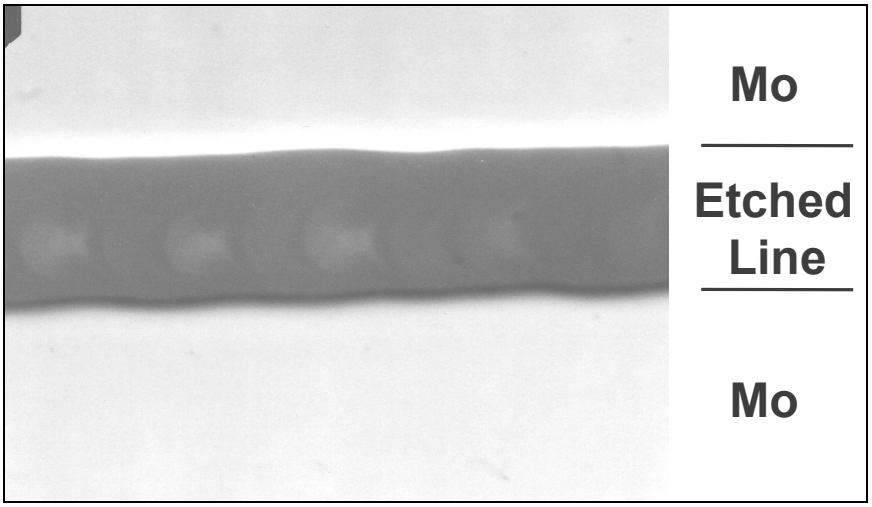


Figure 25. Scribe line produced by the "Jet etching" alternative P1 process (~180 μm wide).

liquid solution directed onto the Mo electrode are scanned across the substrate while a current is passed through the liquid jet. The liquid solution is selected to remove material primarily at the point of electrical contact between the liquid jet and the substrate; the solution is substantially non-reactive in all other areas where there is no electrical enhancement. These experiments were a success from the standpoint of the P1 geometry produced (Figure 25). However, the demonstrated process speed was low and equipment reliability was poor.

During Phase 3, SSI delivered M7 and M8 subcontract deliverables fabricated in the Phase 2 large area reactor and through all subsequent device formation processes as ~30x120 cm circuit plates. After all device fabrication processes, these ~30x120 cm circuit plates were laminated and framed to create 40 W products (ST40) or were cut to smaller sizes to produce smaller products (ST5, ST10). Table 4 summarizes the commercial products delivered to NREL for M7.

Table 4. M7 Contract Deliverables.

Product Power (W)	SSI Product Designation	Quantity Delivered	NREL power measurements (W)
5	ST5	3	5.5 5.6 5.6
10	ST10	3	10.5 11.2 11.2
40	ST40	4	See Figure 27

SSI delivered a second 1 kW set of modules (28 for 1kW array and 2 spares) fulfilling the M8 subcontract deliverable (Figure 26). Large Area Continuous Solar Simulator (LACSS) measurements at NREL are summarized in the distribution chart presented in Figure 27. The NREL measured average efficiency at standard test conditions is 11.4 %. SSI and NREL measurements of these modules agree within 3% when the data is corrected to standard test conditions.

Figure 26. Second 1kW array delivered to NREL under this subcontract (1998).

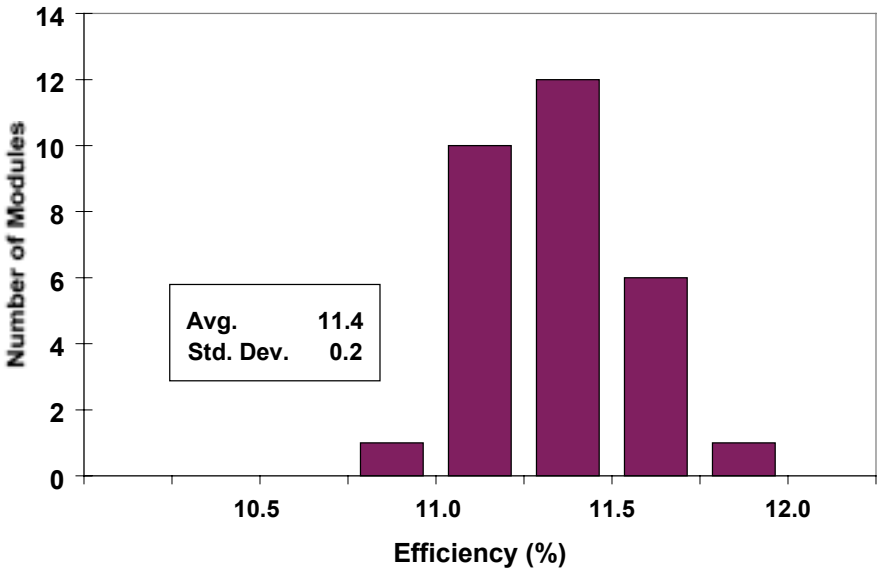


Figure 27. NREL measured efficiency distribution for the 30 modules of the second 1kW array delivered to NREL under this subcontract (28 modules for a 1kW array and 2 spare).

One of these modules achieved an NREL confirmed world-record (1998) 11.8 %, 3651 cm^2 aperture area efficiency (Figure 28).

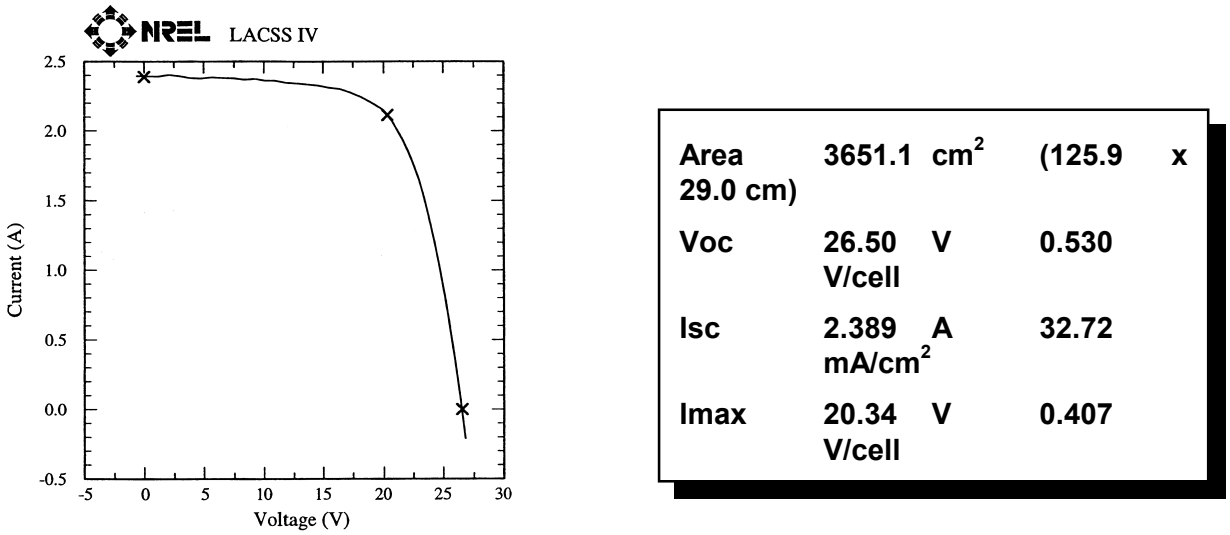


Figure 28. NREL confirmed world-record (1998) 11.8 %, 3651 cm^2 aperture area efficiency module.

Module Reliability and Packaging

Package development

Approaches to package development during this subcontract were largely determined by requirements imposed by absorber formation development efforts. In response to reactor studies under this subcontract, SSI designed and built a new large area reactor. While addressing this issue during the second phase of this subcontract, the baseline reactor was used to produce subcontract deliverables and introductory CIS-based products based on 10x30 cm circuit plates combined to form prototype ~30x120 cm modules, and 5 W and 10 W products. This required defining and demonstrating new package designs to combine 10x30 cm circuit plates in one package.

Figure 29 illustrates the single circuit plate package design used prior to this subcontract for prototype

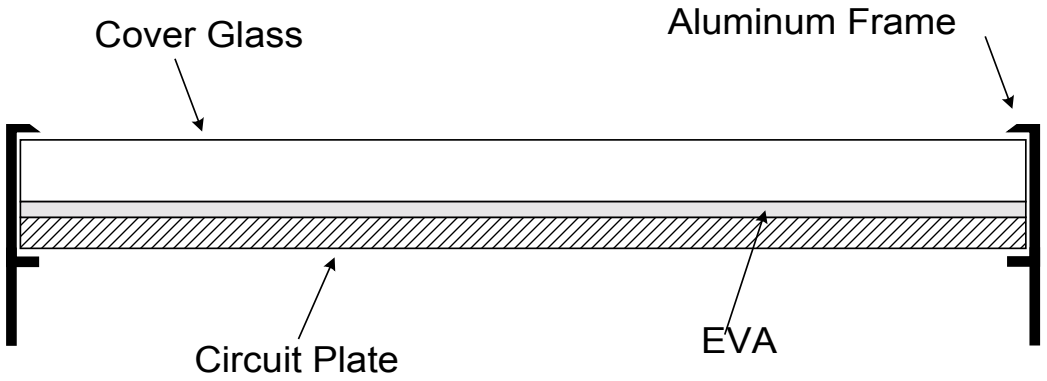


Figure 29. Single circuit plate module configuration.

modules and modules delivered to NREL for 1 kW arrays. Figure 30 illustrates the new package design for combining ~10x30 cm circuit plates to form ~30x120 cm modules, and 5 W and 10 W products. In both cases, EVA is used to laminate circuit plates to a tempered cover glass and the module is framed with an Al extrusion (previous designs also used injected plastic frames). For the package design combining 10x30 cm circuit plates, the addition of a Tedlar/Al/polyester/Tedlar (TAPT) backsheet provides a hermetic seal over the backside of the module.

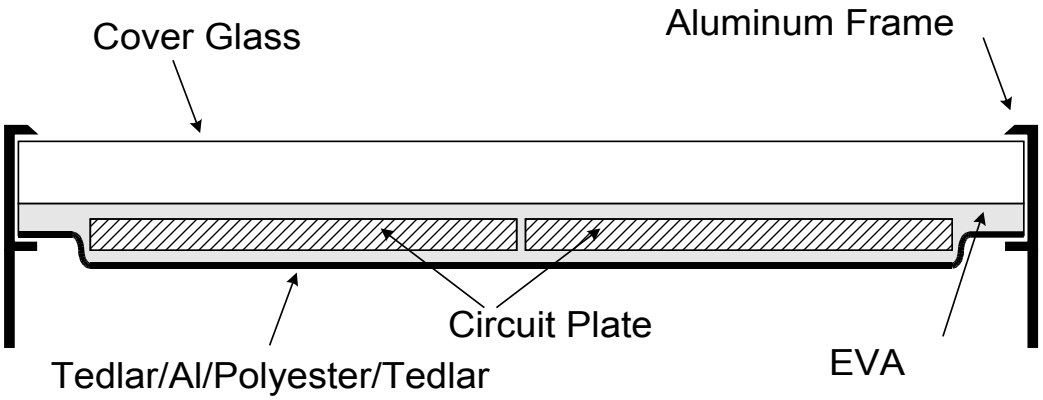


Figure 30. Multiple circuit plate module configuration.

Prior to this subcontract, prototype modules used the single circuit plate module configuration. However, production and product introduction began during this subcontract with the multiple circuit plate module configuration. A module configuration similar to the multiple circuit plate configuration was retained after discontinuing fabrication of products from multiple 10x30 cm circuit plates and beginning processing of only ~30x120 cm circuit plates and smaller plates cut from ~30x120 cm circuit plates. Figure 31 illustrates the module configuration that retains the TAPT backsheet and is presently used for all products and prototype modules. Additional package development efforts are discussed in the following sections as they relate to package development to pass accelerated environmental tests.

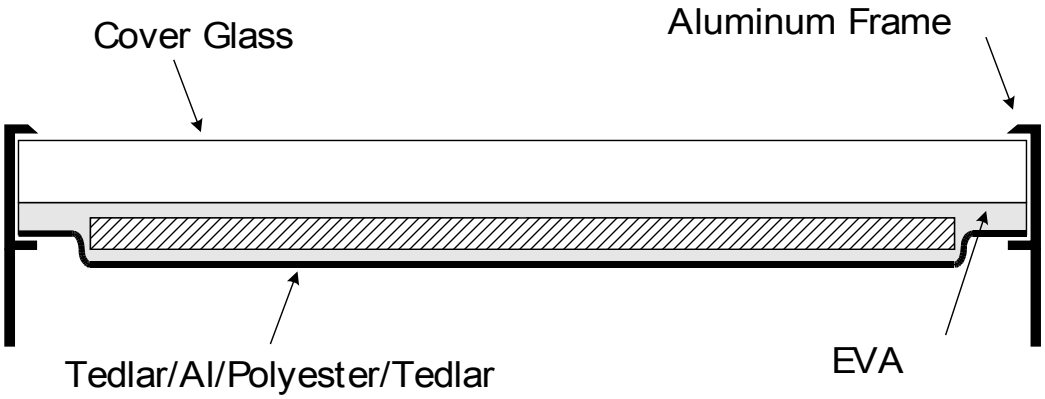


Figure 31. Single circuit plate module configuration with a TAPT backsheet.

The TAPT backsheet covering the edges of the circuit plate provides an edge seal. In addition, removal of the device layers from the edge of the circuit plate is not required for electrical isolation from the frame. Disadvantages of this single circuit plate with a TAPT backsheet configuration include the cost of the TAPT and a second layer of EVA, and increased operating temperature due to the insulating effect of additional layers.

Long-term Outdoor Stability

Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules

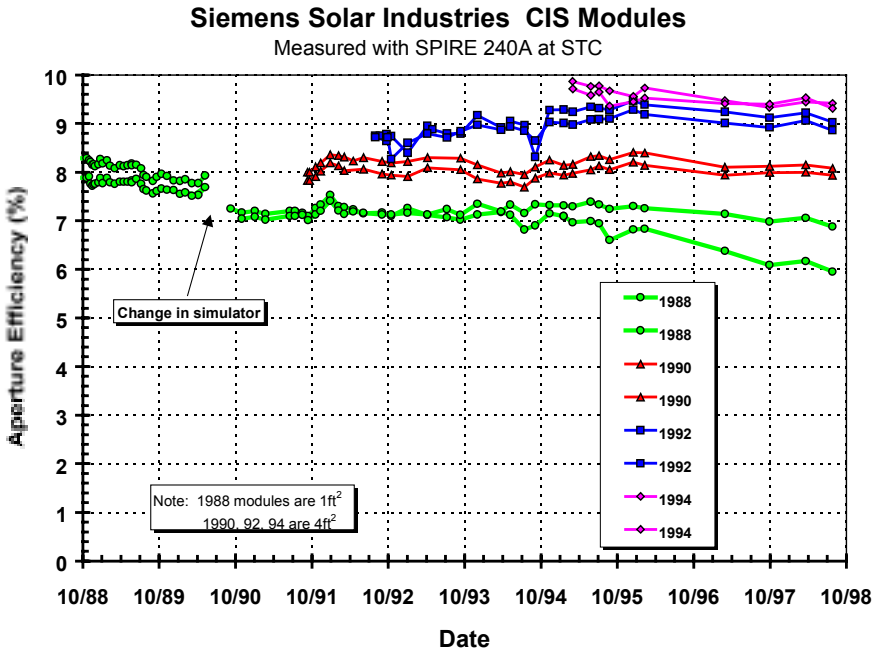


Figure 32. Long term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules have undergone testing for as long as ten years.

have undergone testing for over ten years. These measurements (Figure 32) were made by bringing the modules indoors, performing the measurements under standard test conditions, and then returning the modules to their outdoor test location.

Development of 1kW Arrays

During Phase 2 of this subcontract, SSI delivered a 1 kW set of modules (Figure 12) and an additional 10 modules for testing to NREL, fulfilling the M3 and M4 subcontract deliverables. The 1 kW set of modules replaced an existing 1 kW array based on an older absorber formation technology. The system was installed May 29, 1997 and data acquisition started on June 5, 1997.

Absorbers for the previous array were $Cu(In,Ga)Se_2$ whereas absorbers for this array are a graded absorber including sulfur; $Cu(In,Ga)(Se,S)_2$. Data for these arrays are summarized in Table 5. The newer array has an average module power of 36 watts. NREL reported stable performance and an average efficiency without correction to standard conditions of 7.7% which is a significant improvement over the ~5.7% average efficiency for the previous CIS array (21). Correcting the measurements made

under prevailing conditions to standard conditions yields array power of 1014 W for an unprecedented (1997) average efficiency of greater than nine percent. The computed temperature coefficient for power is -0.44%/°C which is also a significant improvement over the -0.8%/°C temperature coefficient measured for the previous array. These demonstrated improvements in efficiency and temperature coefficient for the newer technology are significant advancements in CIS-based technology.

One of these modules achieved an NREL confirmed world-record (1998) 11.8 %, 3651 cm2 aperture area efficiency (Figure 28).

Table 5. $Cu(In,Ga)Se_2$ and $Cu(In,Ga)(Se,S)_2$ Array Data.

		$Cu(In,Ga)Se_2$	$Cu(In,Ga)(Se,S)_2$
Installed		1993	1997
Power (Corrected to STC)	(W)	865	1014
Efficiency (Corrected to STC)	(%)	6.4*	9.0
Temperature Coefficient	(% / °C)	-0.8	-0.44
Average Module Temperature	(°C)	41	54**
Average Air Temperature	(°C)	17	22**
Number of modules		34	28
Cells per module		53	50

* Calculated based on average Eff and temperature (5.7%, 40.6 °C)

** Data from summer months

For measurement of the 1 kW array, the modules are not brought indoors for IV measurements but rather measurements are made in the field; they are kept under load, and measured every half hour field using automated power trackers. Good stability with no transient effect induced seasonal variation in performance is demonstrated for this temperature corrected data (Figure 33, Figure 34). These studies demonstrate that thermally induced transients, observed after exposure to accelerated environmental

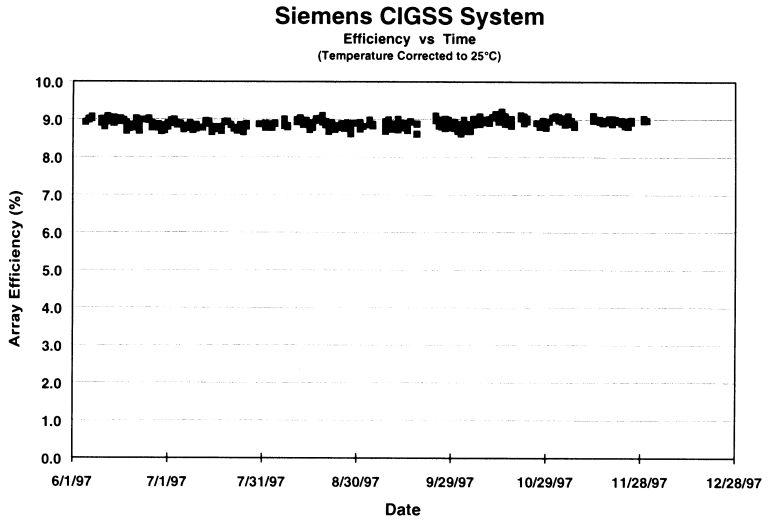


Figure 33. Phase 2 field measurements, power and efficiency, of the 1 kW Cu(In,Ga)(Se,S)2 array delivered to NREL. No photo or thermally induced instability is observed.

testing conditions, are not observed in the field despite daily and seasonal changes in module temperature.

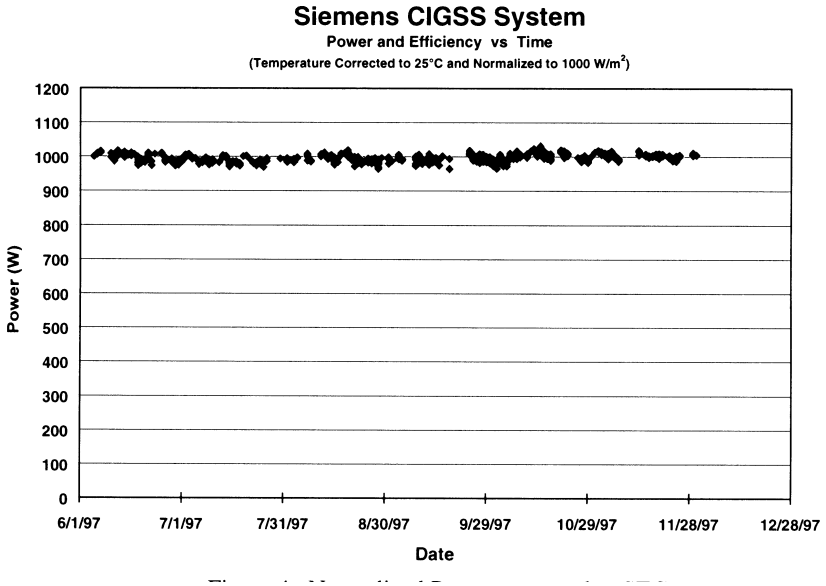


Figure 34. Phase 2 field measurements, power and efficiency, of the 1 kW Cu(In,Ga)(Se,S)$_2$ array delivered to NREL. No photo or thermally induced instability is observed.

Additional data was provided by NREL after decommissioning the modules delivered in 1997 and replacing them with modules installed during 1998 as the second 1kW array delivered to NREL under

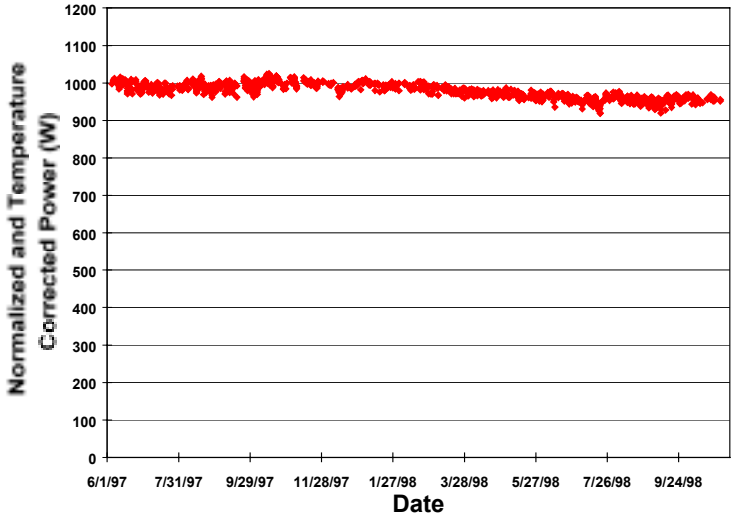


Figure 35. Automated field measurements of the 1 kW Cu(In,Ga)(Se,S)$_2$ array delivered to NREL in 1997.

this subcontract. NREL provides data from array and module measurement based on multiple measurement methods. Measurements on the array delivered in 1997 made in the field using automated power trackers show a change in performance beginning early in 1998 (Figure 35).

In contrast to these results, NREL field measurements of the three strings in the array using a Daystar measurement system indicate no change in array performance (Figure 36).

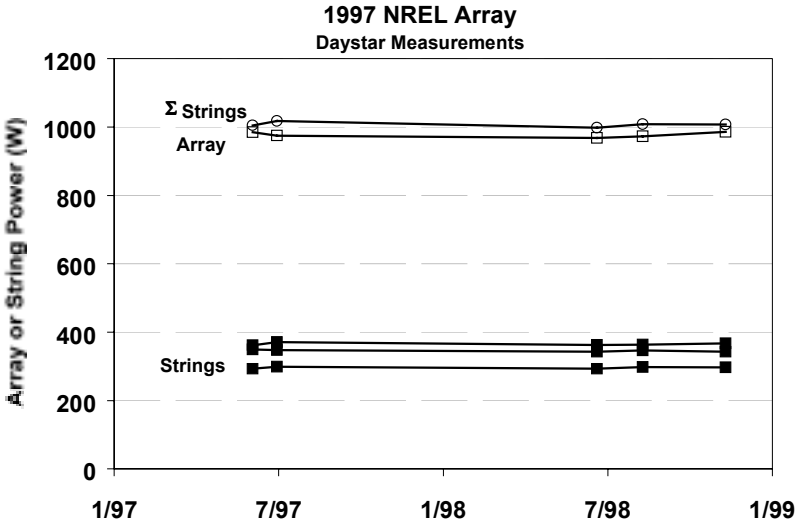


Figure 36. Daystar field measurements of the 1 kW Cu(In,Ga)(Se,S)$_2$ array delivered to NREL in 1997.

Also in contrast with the automated power tracker data, measurements of modules at NREL using the Standard Outdoor Measurement System (SOMS) indicate a change in power shortly after deployment (Figure 37). Differences in the changes in performance for different modules are also observed.

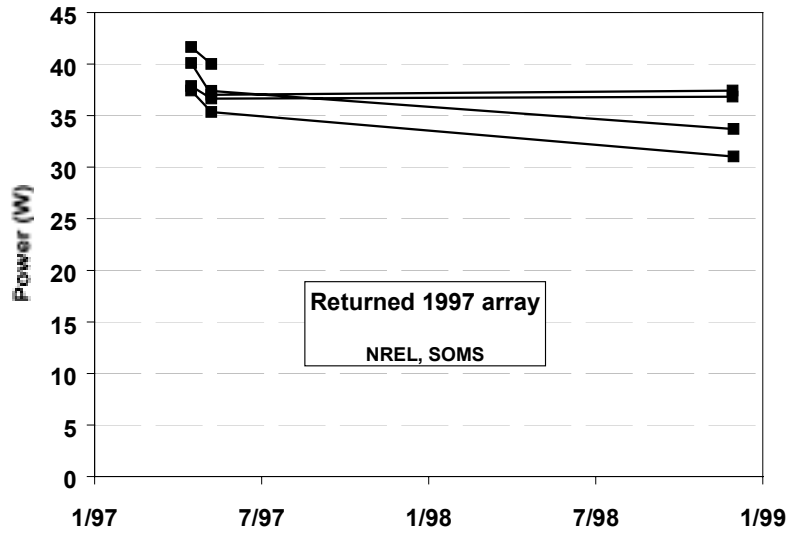


Figure 37. Standard Outdoor Measurement System (SOMS) measurements of modules in the 1 kW Cu(In,Ga)(Se,S)$_2$ array delivered to NREL in 1997.

Some of the differences between these measurements are likely due to the confounding of measurements by transient effects; which is a major topic for the following section of this report. For example, the effects of light exposure history are significant and may confound measurement results. The following chart (Figure 38) portrays module data collected using a Large Area Pulsed Solar Simulator (LAPSS) before and after a relatively short outdoor exposure at SSI after the modules from this array were returned from NREL. The open square data markers are before outdoor exposure and the filled square data markers are after the outdoor exposure. All modules showed significant improvements with light exposure.

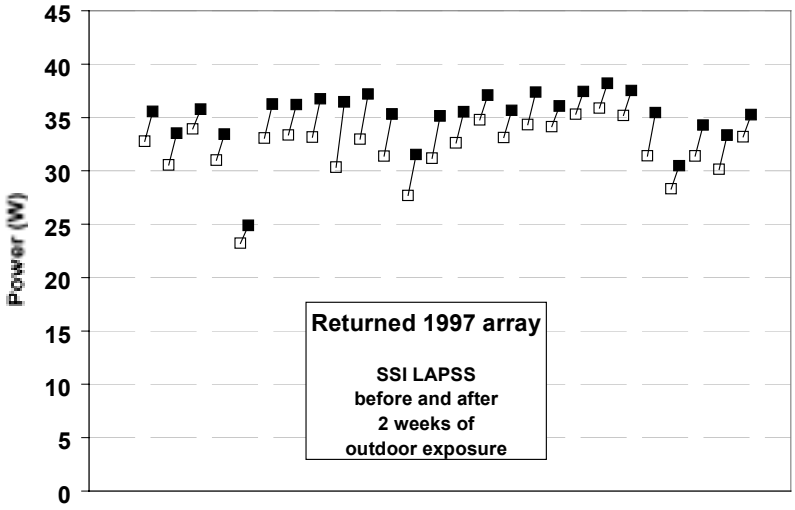


Figure 38. LAPSS measurement of decommissioned modules from the 1997 1 kW array before and after two weeks of outdoor exposure (abscissa – module identifier).

Similarly, the effects of voltage bias history can effect measurements. LAPSS measurements at SSI include a short voltage bias prior to measurement that partially compensates the LAPSS measurements

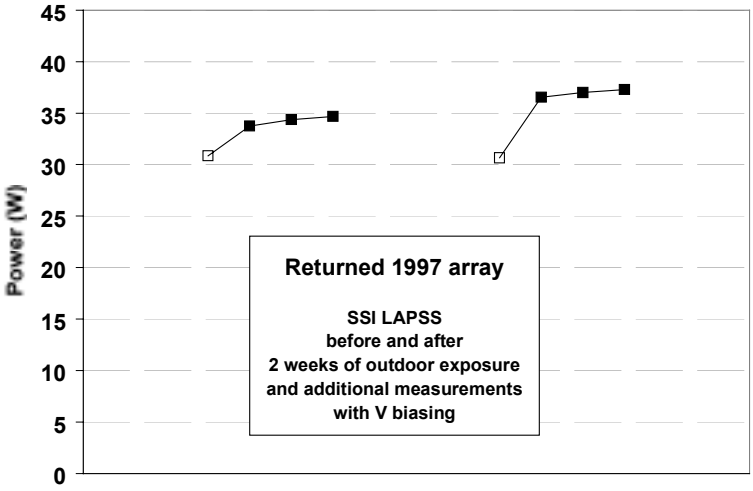


Figure 39. LAPSS measurement of decommissioned modules from the 1997 1 kW array with voltage biasing the standard LAPSS tests (abscissa – module identifier).

and makes them more similar to the higher efficiency measurements obtained using a solar simulator with a continuous light source. Figure 39 illustrates continued improvements in efficiency with additional voltage biasing (filled square data markers) after the short voltage bias of the standard LAPSS test (open square data markers).

These examples of the effects of voltage bias history and light bias history illustrate the difficulty in obtaining data that are not confounded by light bias or voltage bias history. The effect of light soaking and voltage biasing are significant and complicate interpretation of NREL and SSI measurements. However, considering all available data indicates that three modules probably degraded primarily due to a decrease in FF. Visual inspection indicates that the decrease in FF may be due to poor adhesion around P1 and at the edges of the individual ~10x30 cm strips used in this interim module design.

As previously discussed, long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules have undergone testing for over ten years (Figure 32). Also, outdoor stability over more than three years (Figure 40) was demonstrated by the array installed at the NREL OTF prior to this subcontract and decommissioned during this contract at the time the array delivered during 1997 was installed (22). This array was constructed with modules fabricated using the single circuit plate module configuration rather than the interim multiple strip circuit plate configuration. As previously discussed (Figure 37), outdoor testing has begun at the NREL OTF of a 1 kW array with modules fabricated using a modified single circuit plate module configuration.

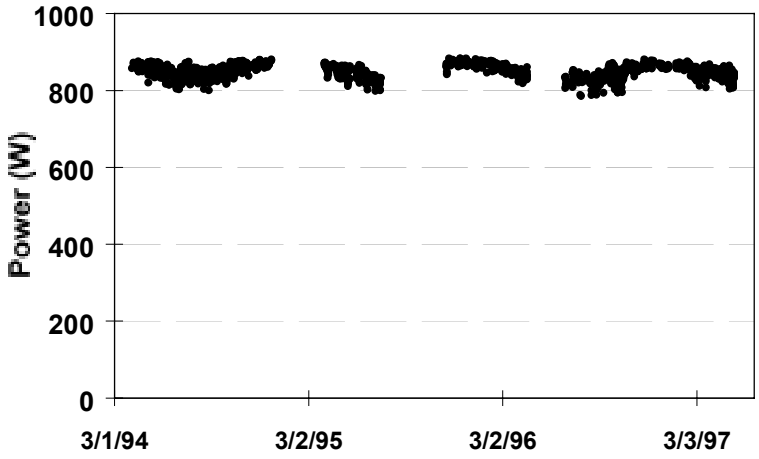


Figure 40. Demonstrated outdoor stability over more than three years for the single circuit plate CIS array installed at the OTF prior to this subcontract and replaced during this subcontract.

Accelerated Testing – including transient effects and process dependence

Laminated mini-modules (M1 deliverables), were subjected to standard accelerated test sequences including thermal cycling (TC), humidity-freeze cycling (HF), and damp heat (DH) exposure at NREL. The sequence of TC and HF testing and measurements was arranged to gain information on the importance of *transient effects* for interpretation of accelerated testing results; the effects of light exposure before, during, and after accelerated environmental testing. Half of the modules went through the TC and HF exposures with an in-situ light exposure of about one sun, and other half were in the dark during the accelerated testing. In contrast, damp heat testing was conducted in the dark only and with

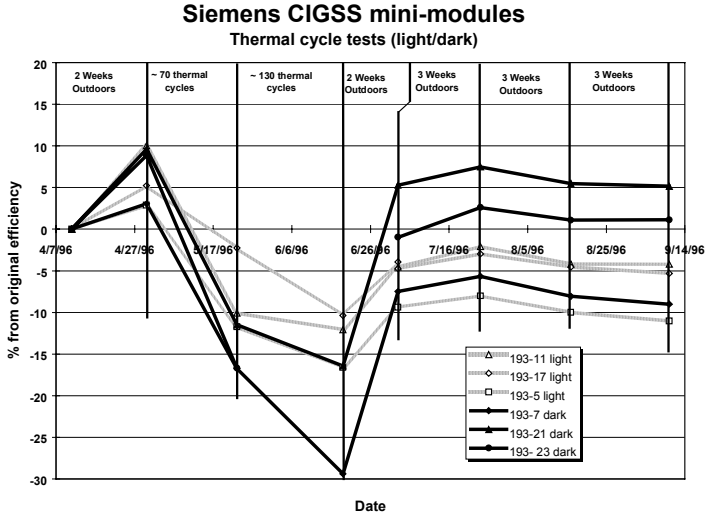


Figure 41. Results of accelerated environmental testing; temporary losses with thermal cycling and recovery with outdoor exposure (NREL testing and measurement).

only two mini-modules. All modules were placed outdoors for at least two weeks before the accelerated environmental testing.

Results for thermal cycling are displayed in Figure 41. With two weeks of outdoor exposure before beginning the accelerated testing, efficiencies improve relative to the measurements made immediately after shipping when the modules were in the dark. Thermal cycling degrades performance by between 10 and 30 points. Less degradation is observed for the group with light exposure during thermal cycling. Performance after subsequent outdoor exposure recovers and the results are similar for the groups with and without light exposure during thermal cycling. Two of the three mini-modules in each group recover to within five points of initial performance.

Results of humidity-freeze cycling are similar to the results for thermal cycling; performance degrades by between 10 and 30 points during accelerated testing, less degradation during cycling is observed for the group with light exposure, and two of the three mini-modules in each group recover to within five points of initial performance. Losses after damp heat exposure are about seventy points with less recovery than for either thermal cycling or humidity-freeze cycling. These mini-modules exhibit fogging around the outside edge that did not disappear with outdoor exposure.

This data set was chosen as an introduction to this section since the data set illustrates the major results to date for accelerated testing, and the dependence of accelerated testing on transient effects (23, 24, 25, 26, 27, 28). SSI fabricated CIS-based modules typically pass the TC and HF accelerated environmental tests when an outdoor exposure is incorporated in the test sequence. Light exposure during these accelerated tests is not adequate to avoid transient effects that are not observed in the field despite daily and seasonal changes in module temperature (Figure 33, Figure 34). Although long-term outdoor stability has been demonstrated at NREL, water vapor ingress resulting from extended damp heat testing permanently degrades performance for most package configures. During this subcontract, SSI has demonstrated packaging designs that protect laminates from water vapor ingress during damp heat testing and allow modules to pass the damp heat test. However, not all modules with these packages pass the development tests and the package designs are not desirable for commercialization.

Transient effects are important for many topics in addition to accelerated testing: process definition, measurement protocols, process predictability, interpretation of experimental results, and understanding of device structures. In addition to the previous examples of the effects of voltage bias history (Figure 39), light bias history (Figure 38, Figure 41), and thermal history (Figure 41), transient effects confound measurements made during module fabrication and final measurements to define product rating. For example, SSI presently includes a light exposure *process step* for both circuit plates before lamination and modules after lamination. The need for this extra process step demonstrates the value of eliminating transient effects. The major discussion of transient effects, including device fabrication process dependencies, is addressed in this section since, in many ways, the confounding of accelerated test results by transient effects delimit subcontract results for environmental studies. It must be emphasized that confounding of test results makes drawing clear conclusions from available data more difficult; however, confounding of test results does not necessarily indicate an inherent problem during normal operating conditions.

Lamination and pseudo lamination experiments have been conducted on mini-modules to determine the potential additional effect of EVA on device performance changes during lamination and other thermal cycling. Thermal exposures during lamination typically produces effects similar to the effects of thermal exposure during accelerated testing. In both cases, the CIS circuit is exposed to much higher temperatures than typical of conditions during normal operation. Circuit plates were laminated with standard lamination procedures and a pseudo lamination procedure where the circuit plates were exposed to the conditions during standard lamination but with a Mylar sheet separating the circuit from the EVA. The following data for this experiment is normalized to the efficiency measured after the standard or pseudo lamination and a standard light exposure. Severe test conditions were selected for this experiment. Mini-modules were continuously held at 85°C since the high temperature exposure section of accelerated tests is thought to be responsible for inducing transient effects. Therefore, a continuous high temperature exposure is a more severe test than cycling between low and high temperatures.

After 939 hours of exposure at 85°C in the dark (Figure 42, Figure 43), the average fraction of the initial efficiency is 84% for laminates. Similar measurements for the pseudo lamination ("Plates" in the following figures) indicate less loss; after the same exposure, the average fraction of the efficiency is 94%. This exposure to 85°C in the dark was extended to 1280 hours with similar results (Figure 43) and the laminated mini-modules were remeasured after about one year outdoors. With an extended outdoor exposure, efficiency for mini-modules after an extended thermal stress is typically within 10% of the initial efficiency. Multiple interpretations of these results are possible: an interaction with EVA, sensitivity to thermal history and inadequate simulation of the actual lamination by the pseudo lamination, or differences in results related to different absorber environments during the exposure at 85°C. Independent of the several possible interpretations of these results, lamination induced losses, even with a potential interaction with EVA, recover with extended outdoor exposure.

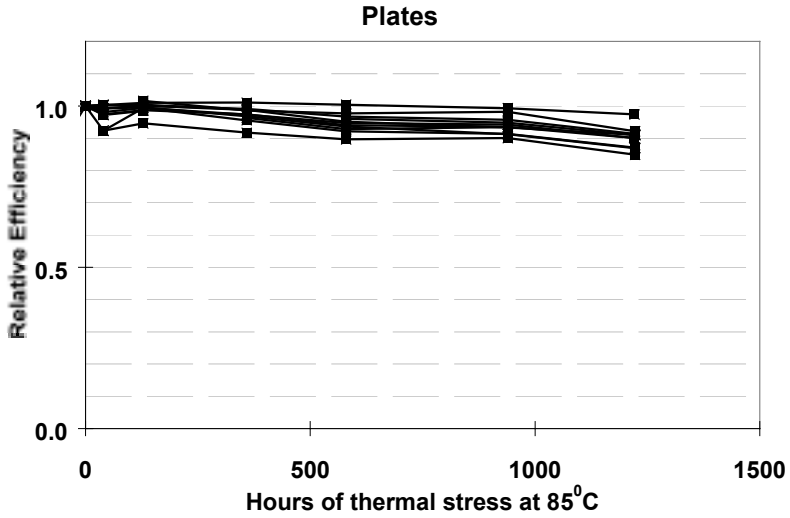


Figure 42 Thermal exposure degradation for pseudo lamination (Plates).

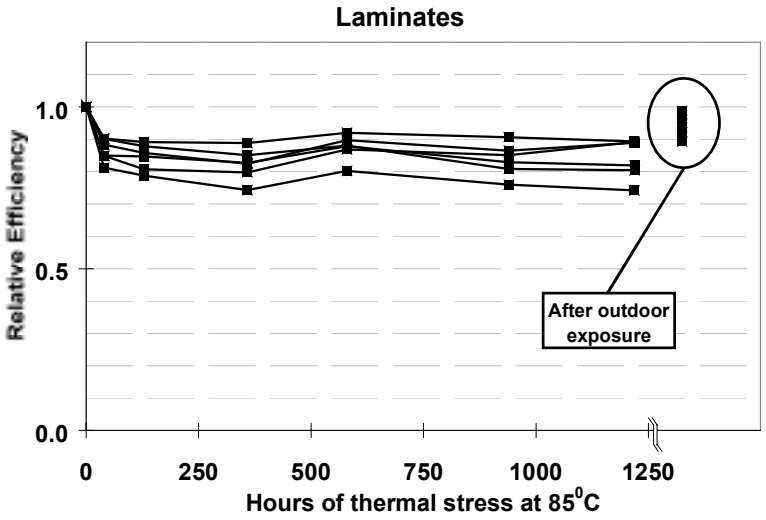


Figure 43. Thermal exposure degradation and outdoor recovery for laminates .

The following further illustrates the confounding effects of transient effects on measurements. A mini-module was measured after outdoor exposure for about six months, and again after storing the mini-module in the dark for about two months. In Figure 44, efficiency is plotted versus light exposure time before ("initial") and after storing the mini-module in the dark. The data at 0.001 seconds was obtained from a pulsed solar simulator and subsequent data was obtained using a solar simulator with a continuous light source. As illustrated in Figure 44, the rate of change with light exposure is dependent on the prior light exposure history.

Improvements with short term exposures of only minutes are observed after an extended period in the dark, even if the module was recently exposed for an extended period. Also, the pulsed light source simulator measurement is significantly lower than the continuous light source measurement.

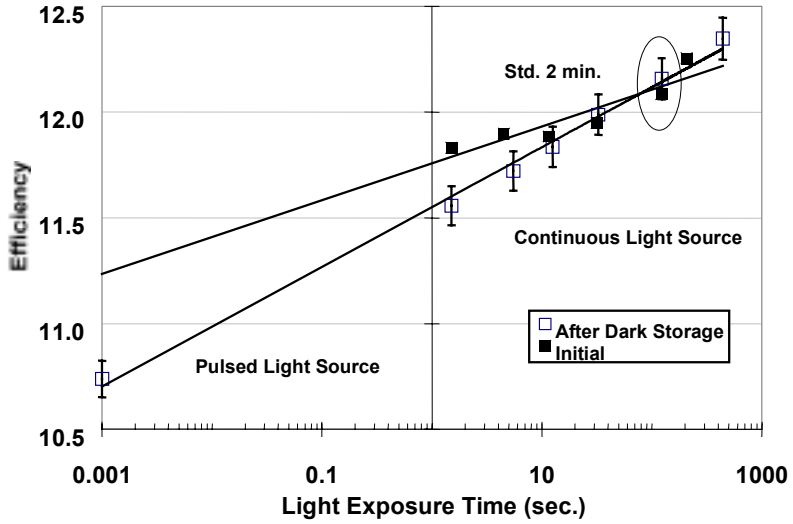


Figure 44. Long term light exposure history affects on the response to short term light exposure.

In a similar comparison, the rates of change of device parameter with light exposure time were compared for one of the modules that were exposed to 85°C in the dark for 1280 hours (Figure 43) and six similar modules that were outdoors for about one year. Increases in efficiency relative to the post lamination

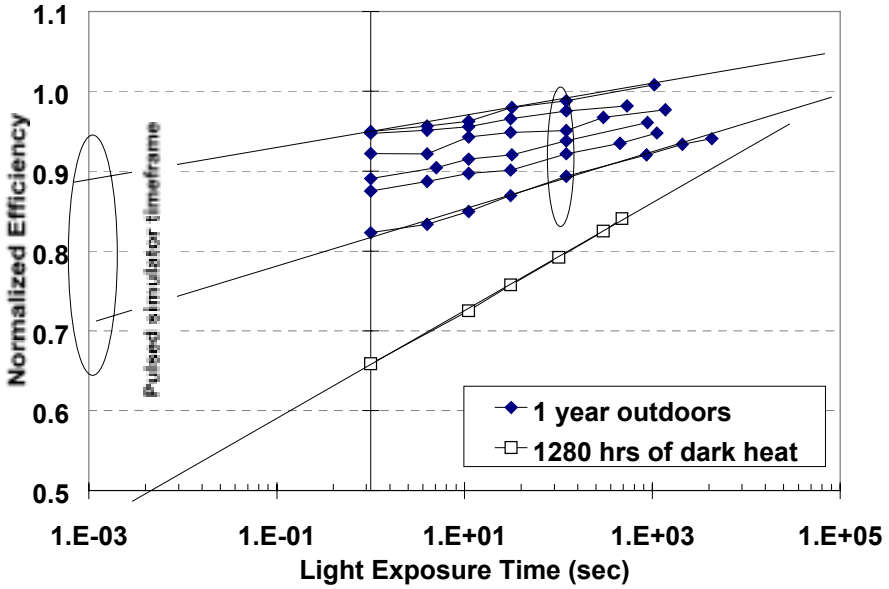


Figure 45. Long term light exposure and thermally induced affects on the response to short term light exposure

efficiency measurement are plotted versus light exposure time in Figure 45. Again, an exposure time of about 0.001 seconds is approximately equivalent to a pulsed solar simulator. Comparing devices with an extended light exposure and with a thermal exposure indicates that both the absolute value of efficiency and rate of change with light exposure are dependent on the thermal and light exposure history. Extrapolating the data for each of the modules that were outdoors to the time of a pulsed simulator test again indicates a wide range of efficiencies for otherwise similar modules. Extrapolation to long light exposure times indicates convergence for modules with similar and dissimilar thermal exposure histories.

These data sets illustrate the potential for error when using a pulsed light source solar simulation to measure module performance when there has been an unusual or ill-defined thermal, illumination, or voltage history. Pulsed light source simulator measurement will typically be significantly lower than continuous light source measurements unless the device under test was very recently exposed to light for an extended period. Also, this difference is not predictable; therefore, it is not possible to define a simple conversion factor to correct a pulsed simulator results to a more appropriate continuous light source standard.

As part of the efforts to first characterize and separate the influence of heat and humidity during accelerated environmental testing, interconnect test structures (Figure 22) were exposed to damp heat

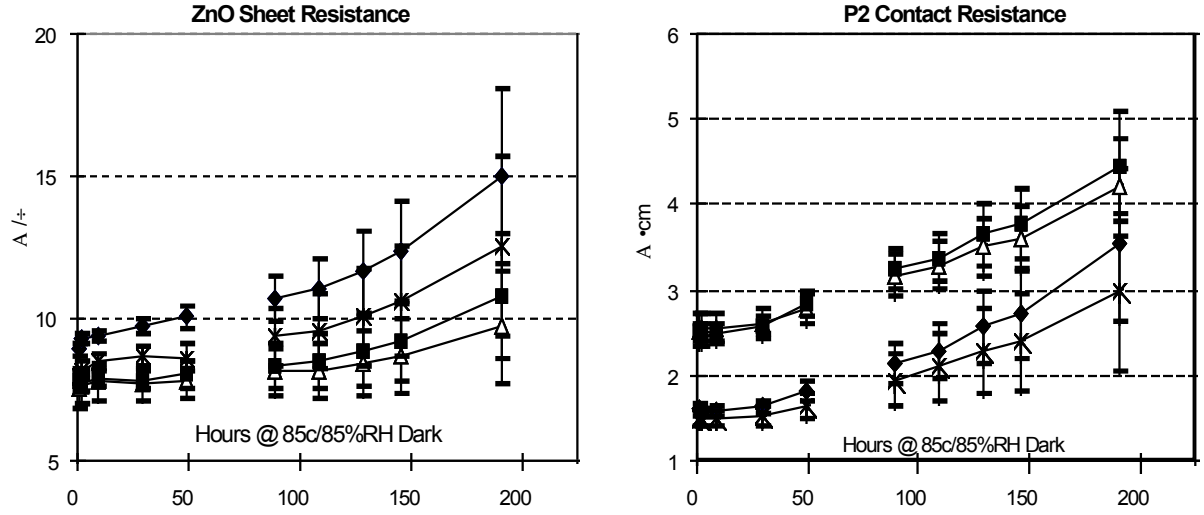


Figure 46. Effects of damp heat testing on ZnO contact resistance and sheet resistance.

(85°C 85% relative humidity). Figure 46 illustrates the effects of damp heat on contact resistance and sheet resistance for four 10x10 cm interconnect test structures laminated but without edge seals. Both parameters increase and the increase correlates with the observation of water penetration into the laminate as indicated by fogging of the EVA.

Additional characterization of the effects of water ingress into laminates, combined with exploration of edge seal options to prevent this water vapor ingress, was performed using laminated 30x30 cm ZnO coated glass plates. These laminates mimic lamination of a large area module but with leads to measure ZnO sheet resistance. Since the package is clear, differences in fogging can be observed and correlated with differences in water vapor ingress for various edge seal options. Relative sheet resistance versus time of exposure to damp heat conditions is plotted in Figure 47. Edge seal options that significantly decrease water vapor ingress have been demonstrated.

Two of these experimental laminates were exposed to outdoor light and the ZnO sheet resistance decreased to nominally the values prior to exposure to damp heat (Dashed lines in Figure 47). This improvement in ZnO sheet resistance is not accompanied by a significant decrease in fogging of the EVA. These results indicate that the effect of water vapor on ZnO sheet resistance is at least partially reversible.

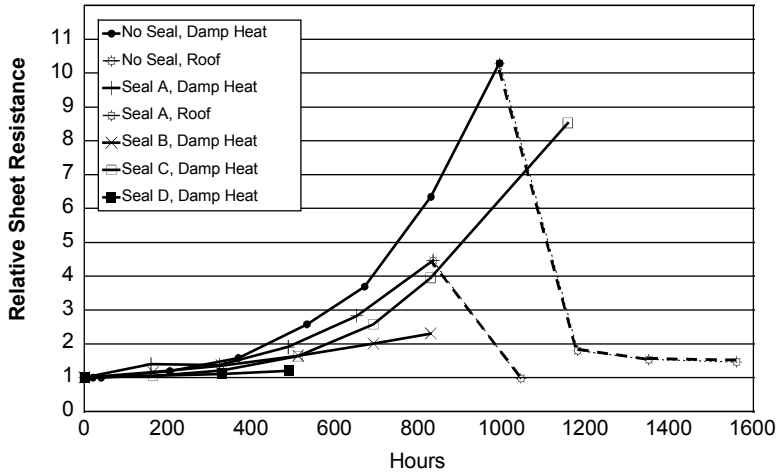


Figure 47. Increases in ZnO sheet resistance with exposure to water vapor and decreases in ZnO sheet resistance with outdoor exposure.

Permanent degradation due to water vapor ingress resulting from extended damp heat testing of EVA based mini-modules is typical. However, a 10x10 cm circuit plate laminated using EVA between an oversized sheet and an aluminum back sheet (TPAT), and including an edge seal, was exposed to 1000 hours of damp heat and subsequently to over 100 days of outdoor exposure. Efficiency dropped by about

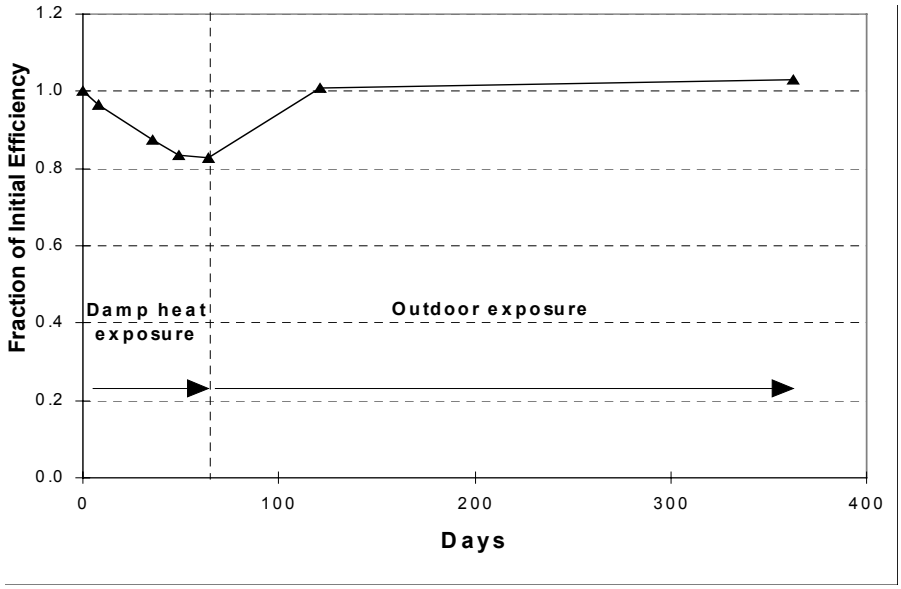


Figure 48. 1000 hour damp heat testing followed by outdoor sun-soaking of an EVA based mini-module.

20% relative to the initial efficiency with the exposure to 1000 hours of damp heat. Outdoor exposure resulted in complete recovery (Figure 48). This result demonstrates that CIS-based devices encapsulated using EVA in a package designed to avoid or minimize water vapor ingress can pass the 1000 hour damp heat test after sufficient outdoor sun-soaking.

Also, SSI has previously demonstrated packaging designs similar to thermopane windows that protect laminates from water vapor ingress during damp heat testing and allow modules to pass the damp heat test. The thermopane design consists of a cover plate separated from the circuit plate by supports at the edges, a desiccated volume of gas between the circuit plate and cover plate, and an edge seal consisting of aluminum foil with a butyl rubber adhesive. Data illustrating these results is presented in Figure 49.

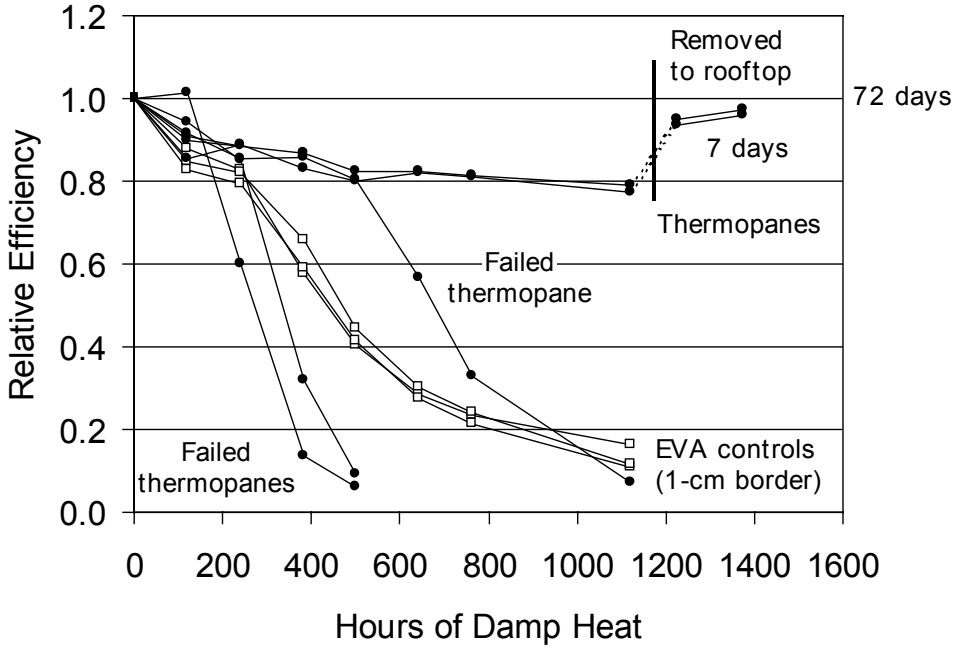


Figure 49. Damp heat exposure followed by outdoor exposure for thermopane and standard EVA encapsulated mini-modules.

Two mini-modules passed the 1000 damp heat test after outdoor exposure while other mini-modules with this design and EVA encapsulated mini-modules failed the test. Also, if the thermopane design fails it tends to fail catastrophically.

Multiple packaging designs with and without EVA have been demonstrated that protect laminates from water vapor ingress during damp heat accelerated testing. Accelerated environmental tests can be passed when an outdoor exposure is incorporated in the test sequence to reverse thermally induced transients effects. Although mini-modules with extremely wide borders and edge seals, or the thermopane design, have passed the damp heat test, the yields were typically low and the package designs are not desirable for commercialization.

These results have been extended using large parts with edge seals and package design options based on replacement of the EVA. To date, these experiments have been based on a relatively small number of test devices in each experimental group and have been confounded by transient effects. Studies have been performed using larger circuit plates since water vapor ingress is related to perimeter length while

degradation is related to circuit area. Unfortunately, large circuit plates and laminates can not be measured using SSI's continuous light source simulator. Uncertainty in both initial and final measurements using SSI's large area pulsed solar simulator have confounded the results. Interpretation of these results is also difficult since the period for recovery with outdoor exposure after accelerated testing is uncertain and may be quite long.

Preliminary results indicate that transients introduced by long term exposure at 85°C or temperature cycling are reduced by soft encapsulating materials such as silicone grease, two part silicone, or partially cured EVA. Also, thermally induced transients may be decreased by replacing the rigid tempered glass front sheet with an elastic material. As with the interruption of previous pseudo lamination experiments, multiple explanations of these results are possible: interactions between EVA and the circuit plate, sensitivity to thermal history and differences between the thermal history for the standard lamination and the alternative laminations, or differences in results related to different absorber environments during the exposures at 85°C. Differences in stress induced during thermal exposures is one model that fits within these possibilities and is supported by the preliminary data. Distinctions between the results of these experiments and previous pseudo lamination and thermal exposure experiments may also be related to changes in the circuit plate fabrication process. Differences in the sensitivity of circuit plates to thermal stresses are induced by differences in the environment during transportation of circuit plates between process steps (discussed below). An additional prototype module with a design that could conceivably be acceptable for production has passed the damp heat test; acceptable loss of only ~2% has been demonstrated for one 18x30 cm glass/silicone/circuit/TPAT structure with edge seals and desiccant incorporated in the package.

Thermally induced transient effects do not necessarily cause modules to fail accelerated environment tests if the thermal stress is followed by an outdoor exposure. However, results presented in this section demonstrate that thermally induced transients are undesirable: product measurements are confounded, two light exposure *process step* have been added, package development is delayed by the requirement to expose modules outdoors for significant periods, and package development is confounded, particularly for large area devices, by measurement uncertainties. Device fabrication dependence of transient effects has been explored to mitigate the effect of transient effects and gain understanding of device structures and performance.

Studies to date have demonstrated no transient effect dependence on relatively minor changes to the present circuit fabrication process with the exception of storage in an inert environment (discussed below). For example, devices made using two Mo deposition processes were measured after initial fabrication, lamination, 20 hours of exposure to 85°C in the dark, and after outdoor exposure for about one week (Figure 50). No statistically significant difference between the two Mo deposition processes was observed for thermal stress or recovery with light exposure. Similarly, no statistically significant difference has been observed for varied glass preparation conditions.

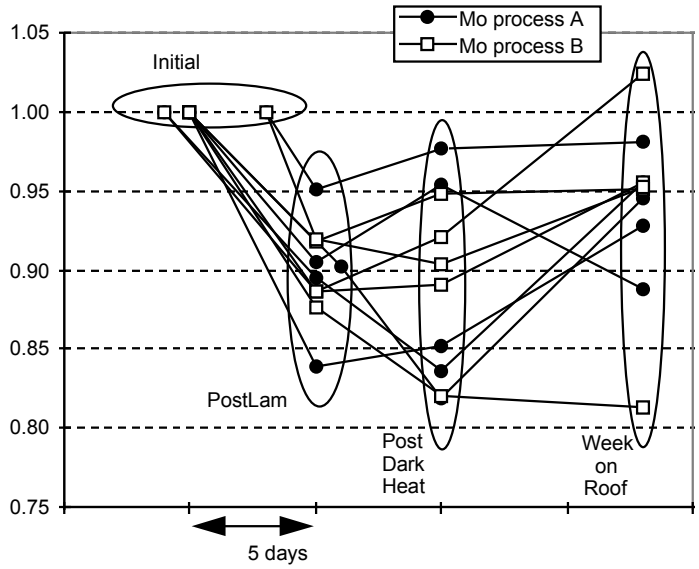


Figure 50. Normalized efficiency for mini-modules fabricated using two Mo deposition process and then exposed to thermal stress and light exposure.

Lower lamination losses as measured using a pulsed simulator have been measured as a function of the exposure time of circuit plates to air during the final stages of fabrication. As illustrated in Figure 51 for

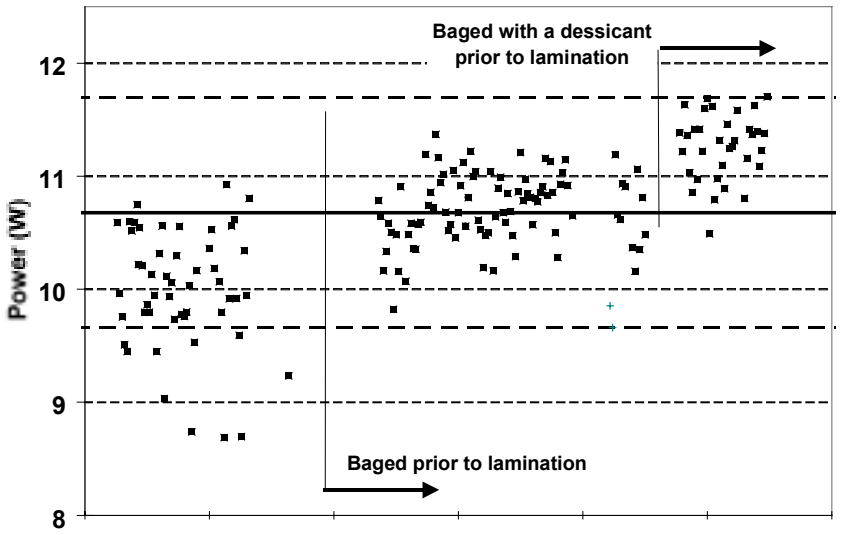


Figure 51. Module power versus atmosphere during transportation and storage (abscissa - module identifier).

9x30 cm circuit plates, lower lamination losses are demonstrated for transporting circuit plates in a bag and in a bag with desiccant as *added process steps.* These added process steps are in addition to the two light exposure process steps for testing before and after lamination. It is not known if this lower

lamination loss for less exposure of circuit plates to air would be observed after extended outdoor exposure.

Additional experiments were conducted using the 10x10 cm mini-module baseline process to characterize the sensitivity of circuit plates to humidity at various stages of the module fabrication process and to determine appropriate circuit plate transportation criteria. Sensitivity to humidity was explored for circuit plates transported under environmentally controlled conditions between the absorber formation and CdS deposition process steps, and between the CdS deposition and ZnO deposition process steps. Otherwise, standard transport conditions were employed. Three environmentally controlled conditions for part transportation were explored: 1) N_2 purge, 2) N_2 purge with desiccant, 3) humidified to ~75% relative humidity. Standard thermal stress test sequences were defined to maximize thermally induced losses and thereby increase the probability of identifying correlation with process conditions. For these experiments, 10x10 cm mini-module were held at 85° for 157 hours without cycling the temperature. Device parameters were measured before lamination, after lamination, and after the thermal stress.

Figure 52 presents data for transportation of circuit plates under controlled conditions between the absorber formation and CdS deposition process steps. Circuit plate performance and module performance, both after lamination and after the thermal stress, is lower for circuit plates that were transported in a humidified atmosphere. Normalizing the data (Figure 53) indicates that both the circuit

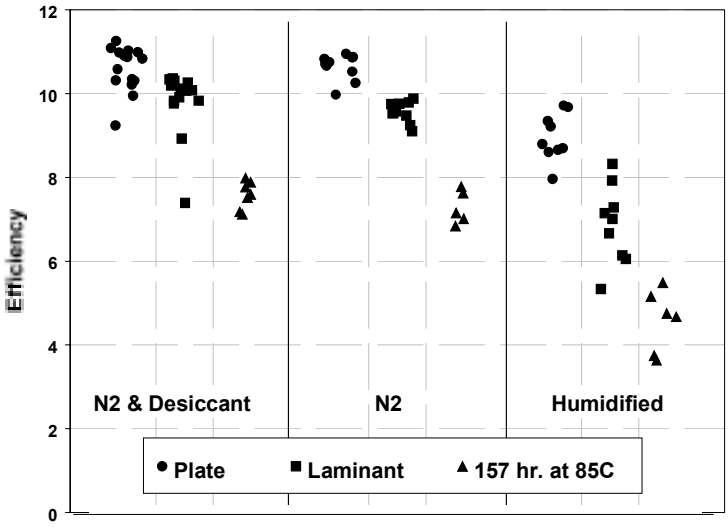


Figure 52 Eff sensitivity to humidity for circuit plates transported under environmentally controlled conditions between the absorber formation and CdS deposition processes.

plate efficiencies and the relative transient losses induced by lamination and the thermal stress are higher for circuit plates that were transported in a humidified atmosphere. Performance differences are primarily due to differences in fill factor.

Correlation was also found between the duration of the circuit plate exposure to a humidified atmosphere and performance before lamination, after lamination, and after the thermal stress. A chart of normalized circuit plate efficiency versus duration of exposure to a humidified atmosphere is presented in Figure 54. The normalization factor is the average efficiency of the group transported with a N_2 purge. Similar results but with less sensitivity to humidity were found for circuit plates transported under environmentally controlled conditions between the CdS deposition and ZnO deposition process steps.

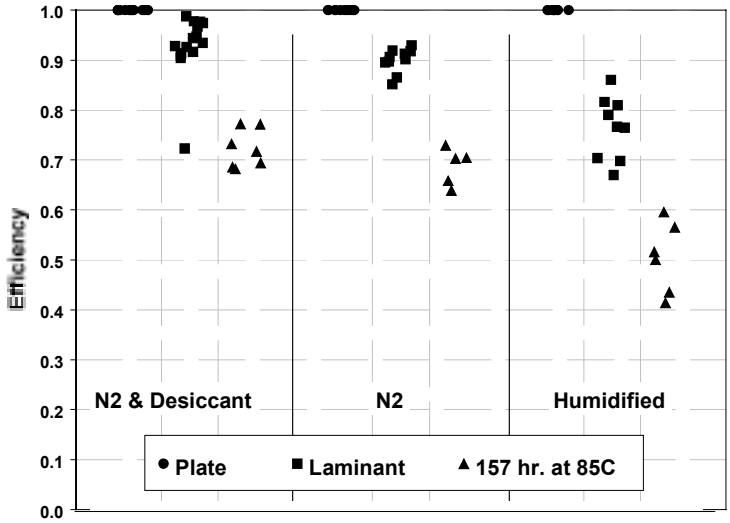


Figure 53 Eff (normalized) sensitivity to humidity for circuit plates transported under environmentally controlled conditions between the absorber formation and CdS deposition processes.

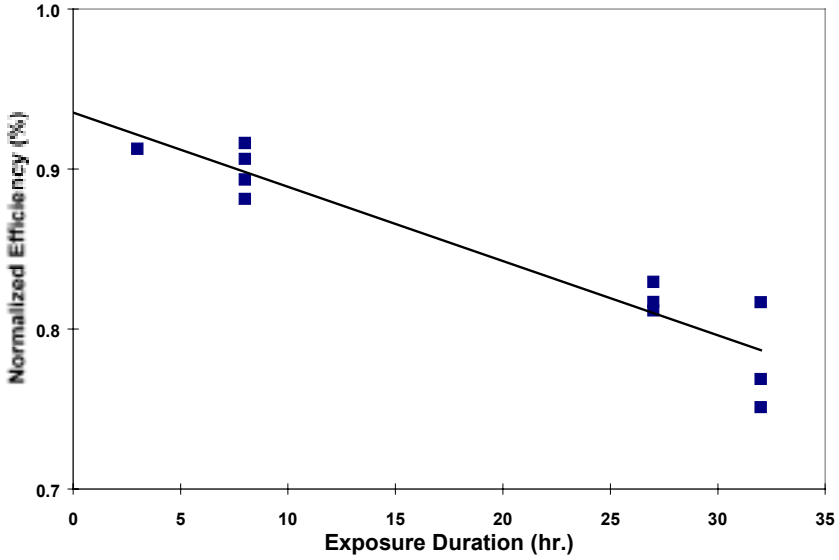


Figure 54. Normalized circuit plate efficiency versus duration of exposure to a humidified atmosphere.

The dependence of transient effects on more extensive changes to the present circuit fabrication process has been examined in collaboration with NREL TFPPP Teams and as studies at SSI extending results from Team activities. SSI's participation in Team activities is focused primarily on understanding the fundamental mechanisms responsible for transient effects in CIGS-based devices with the objective of

eliminating or minimizing their impact. The NREL TFPPP "Transient Effects Group" is composed of representatives from industry, NREL and universities (Keith Emery, NREL; Larry Olsen, WSU; James Phillips, University of Delaware; James Sites, Colorado State University; Dale Tarrant, Siemens Solar Industries; Hong Zhu, Penn State University). Although this report does not attempt to summarize the results for all of the extensive team activities, the following results, observations, and areas of research related to transient effects illustrate the work of the group:

- Changes in FF dominate changes in IV characteristics for thermal stress and light exposure.
- Changes in "series resistance" account for these changes in FF where the term "series resistance" may also include "roll-over" effects (decreasing rather than increasing slope of the current versus voltage curve for increasing voltage).
- Capacitance versus voltage measurements (in the dark) demonstrate a decrease in hole density with thermal exposure.
- Light exposure after a thermal exposure increases the hole density to approximately the concentration prior to thermal exposure.
- Differences between current versus voltage characteristics with and without illumination (dark IV versus light IV) are particularly dramatic for the thermally stressed state.
- Although the changes in series resistance and hole density with thermal and light exposure are about the same magnitude, causality has not been demonstrated.
- Differences in the rate of recovery for four illumination spectra suggest that the recovery process may be dependent on the spectrum of the illumination.
- Since the rate of recovery is similar for no illumination and for illumination with red light, the recovery process may depend on absorption in the window layer or in the near surface region of the absorber.
- The transient effects are not solely a lamination effect – observations made on unlaminated devices are consistent with measurements made on laminated mini-modules.
- SSI and Larry Olsen's group at Washington State University demonstrated light induced transient effects for SSI absorbers with and without buffer layers.
- Device modeling software (AMPS, Penn. State) was applied to the study of transient effect and the insights gained from these studies are being applied to further understanding of the role of device structures in the expression of transient effects.
- The Transient Effects Group confirmed decreases in transient effects with SSI process changes to reduce exposure to humidity during module processing.
- The amplitude of transient effects is dependent on many factors including absorber/buffer/window combinations, absorber surface modification, SSI processing such as exposure to humidity, thermal history, illumination history, and voltage bias history.
- Minimal transients were demonstrated for a WSU buffer layer formation process.

The importance of process steps, particularly alterations to the buffer layer or CIS surface is illustrated by the results of collaborations between SSI and Washington State University. SSI demonstrated and presented data to the National CIS R&D Team on increases in performance with light exposure for devices with no ZnO. Based on these results, SSI and Larry Olsen's group at WSU conducted studies to explore the role of the CdS buffer layer and the connection between buffer layers and light induced transient effects. SSI graded absorbers were processed by SSI and WSU with and without buffer layers and with and without degreasing and a combination of degreasing and a KCN surface treatment.

Efficiencies were improved by the degreasing and KCN etch. Light exposures of 3 and 13 hours improve performance (Figure 55): 20 to 50% with CdS, saturating after 3 hours, 200 to 250% without CdS, continuing after 3 hours. With CdS, efficiency improvements were due to increases in FF. Without

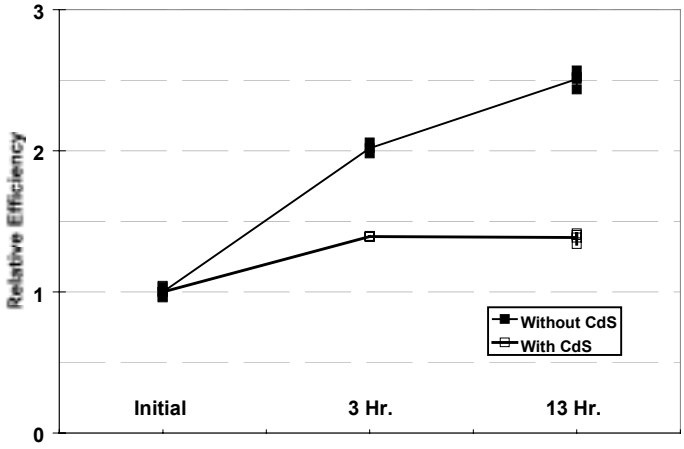


Figure 55. Relative efficiency versus light exposure time for mini-modules with and without a CdS

CdS, efficiency improvements also included improvements in Voc, Jsc and FF. With extensive light exposure, the performance of devices without a buffer layer approaches the performance of devices with a buffer layer. A rollover of forward bias current (i.e. decreasing rather than increasing slope of the current versus voltage curve for increasing voltage) is observed for all but the case of degreasing combined with a KCN etch. This data implies that rollover is associated with CIS surface conditions and interactions of the ZnO and CdS with the CIS surface. Combining these observations regarding light induced transients with or without a buffer layer and the results from the Transient Effects Group regarding changes in hole density with light exposure implies that mechanisms responsible for transients and the role of buffer layers are related and that both induce changes in the absorber.

NREL National CIS R&D Team activities (Present Junctions Group) have also included studies to elucidate the function of the CdS buffer layer, causes for device performance dependence on buffer layer deposition technique, and the function of components of the CBD bath for deposition of CdS. These topics are of particular interest to SSI since they relate to understanding of CIS device performance. In light of results relating transient effects and surface preparation, these studies are also potentially important for understanding the connection between the buffer layer and light induced transient effects.

The following SSI results extend the studies of the Present Junction Group to the topic of transient effects. A "Partial electrolyte" (PE) solution is defined by the TFPPP CIS Team as the CBD deposition process for CdS but without thiourea in the bath. CdS is not deposited by this solution. SSI fabricated mini-modules with the following combinations of treatments augmenting or replacing the CdS deposition process with a Cd partial electrolyte solution (CdPE):

- CdPE treatment and then CBD CdS
- CBD CdS ("baseline")
- CdPE only
- No treatment and no CdS

Similar treatments were performed to explore analogous treatments based on zinc rather than Cd. A "ZnPE" was prepared using the recipe for the CdS "PE" but with the substitution of a zinc salt for $CdSO_4$. SSI fabricated mini-modules with the following combinations of treatments augmenting or replacing the CdS deposition process with a Zn partial electrolyte solution (ZnPE):

- ZnPE treatment and then CBD CdS
- CBD CdS ("baseline")
- ZnPE only
- No treatment and no CdS

Results of these experiments are presented in two chart types for each of the two partial electrolyte types. Mini-module parameters were measured at standard test conditions while tracking device performance as the mini-modules were continuously exposed during testing. Mini-module parameters were measured at approximately 1.5, 5, 12, 30, and 120 seconds. The first chart type presents efficiency data measured after 120 seconds of exposure for each treatment. Horizontal lines indicate the lower control limit (LCL), average efficiency (Avg.), and upper control limit (UCL) for the contemporary baseline process. The second chart type presents the efficiency data for each measurement (1.5, 5, 12, 30, and 120 seconds) of each mini-module normalized to the first measurement at ~1.5 sec. Five connected data points present the performance versus exposure time data for each mini-module.

Data in Figure 56 for the CdPE indicates that mini-module performance (after two minutes of exposure) with only the CdPE treatment and with the combined CdPE treatment and CdS deposition are similar to the performance for "baseline" mini-modules with the standard CdS deposition. Only the untreated circuits exhibit inferior performance due to low FF. It might be argued that the mini-modules that received only the CdPE treatment exhibit systematically higher Voc and Eff, however this result is not demonstrated statistically because of the small number of parts in each group.

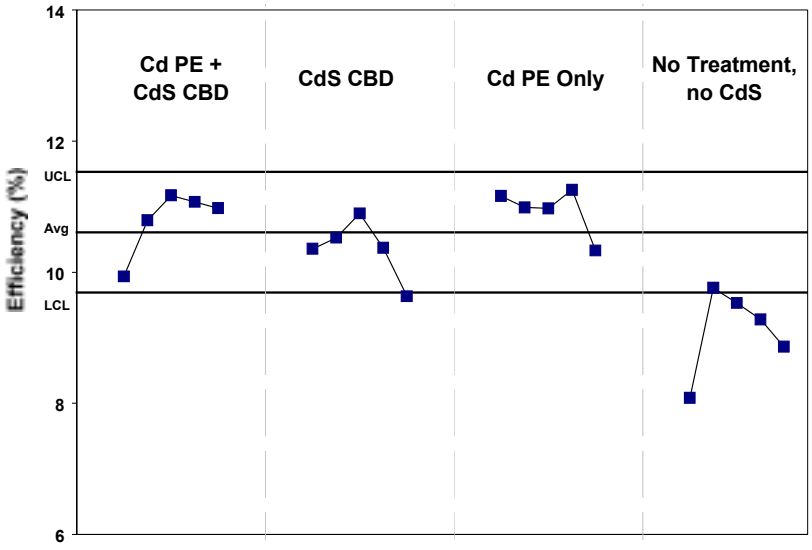


Figure 56. Mini-module efficiency for various combinations of Cd partial electrolyte (CdPE) treatment and CBD CdS depositions (abscissa - module identifier).

The normalized efficiency data, including data for each measurement while the mini-modules are exposed (Figure 57), indicates that light induced transients are greater without CdS and that the combination of CdPE treatment and then CBD CdS may decrease light induced transient effects.

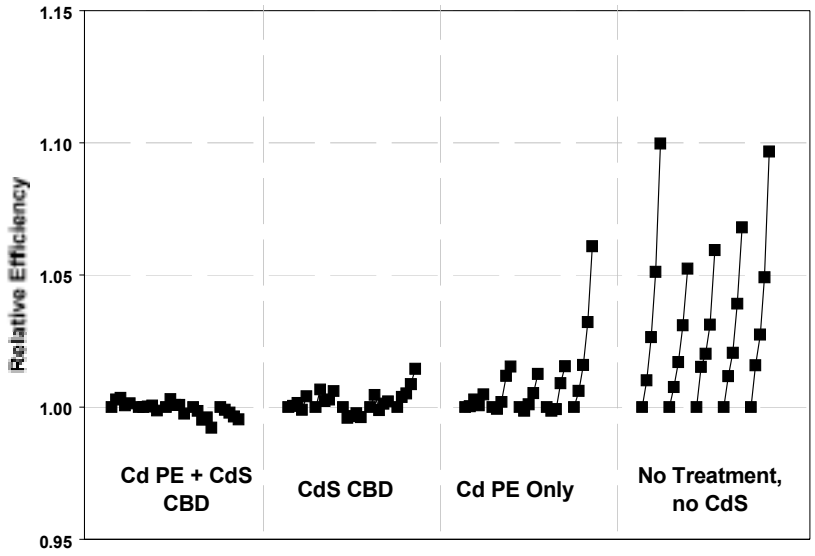


Figure 57. Normalized mini-module efficiency at 1.5, 5, 12, 30, and 120 sec. of illumination for various combinations of Cd partial electrolyte (CdPE) treatment and CBD CdS depositions (abscissa - module identifier).

In addition, the impact of these treatments on thermally induced transients was explored by laminating these mini-modules and exposing them to 85° for 123 hours. Untreated mini-modules and mini-modules that received only the CdPE treatment exhibit higher thermally induced transients than mini-modules with baseline CdS or the combined CdPE treatment and CdS deposition.

The data set related to the ZnPE indicates that mini-module performance (after two minutes of exposure) with the combined ZnPE treatment and CdS deposition are similar to the performance for "baseline" mini-modules with the standard CdS deposition (Figure 58). The untreated circuits and circuits with only the ZnPE treatment exhibit significantly inferior performance due to low Voc and FF.

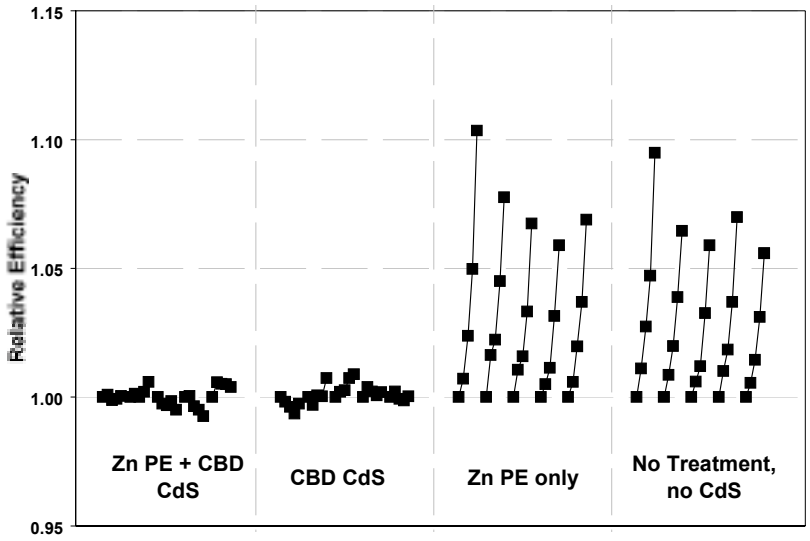


Figure 58. Mini-module efficiency for various combinations of Zn partial electrolyte (ZnPE) treatment and CBD CdS depositions (abscissa - module identifier).

The normalized efficiency data, including data for each measurement while the mini-modules are exposed (Figure 59), indicates that light induced transients are greater for both treatment types that do not deposit CdS.

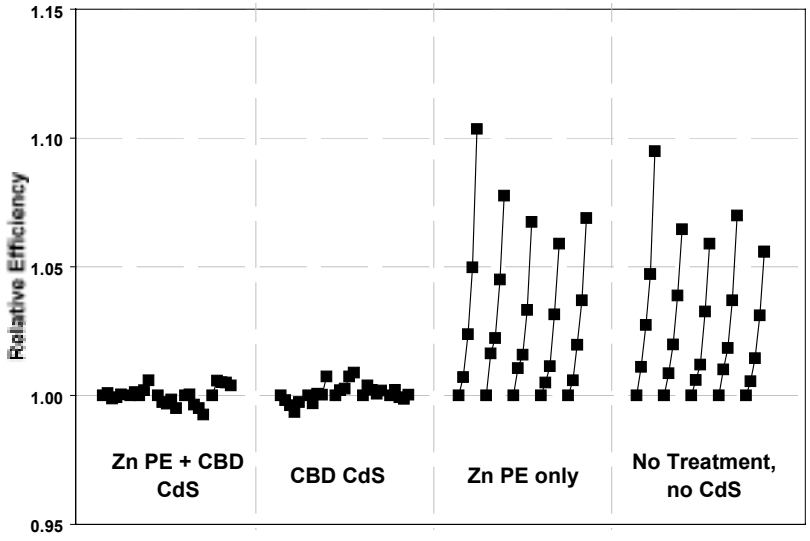


Figure 59. Normalized mini-module efficiency at 1.5, 5, 12, 30, and 120 sec. of illumination for various combinations of Zn partial electrolyte (ZnPE) treatment and CBD CdS depositions (abscissa - module identifier).

Conclusions

Outstanding progress toward achieving NREL/DOE goals was achieved during this subcontract:

- Initially, a 10x10 cm substrate size baseline process was repeatedly executed. The Statistical Process Control methodology was applied and rigorously demonstrated process reproducibility and yields.
- Understanding of the importance of materials of construction and the physical layout for absorber formation reactors was realized.
- Based on this understanding, SSI designed and built a replacement large area reactor based on a more direct scale-up of the baseline reactor.
- While designing and building the new large area reactor, SSI accomplished the task of defining and demonstrating new package designs to combine 10x30 cm circuit plates (produced in the small baseline reactor) into one package.
- This new package design allowed delivery of large area prototype modules to NREL for evaluation, and the introduced the first CIS-based *products* – 5 watt (ST5) and 10 watt (ST10) modules.
- After completion of the new large area reactor, all processes were scaled to a ~30x120 cm plate size. Subsequently, only large ~30x120 cm circuit plates were fabricated for ~30x120 cm prototype modules or, after cutting the large circuit plates into smaller circuit plates, for the two new CIS-based products.
- The scaled process exhibits generally good control for extended periods with periodic shifts in the short-term process average that appears to result from batch-to-batch variability in precursor or base electrode preparation. Similarly, periodic shunting along the laser scribed pattern lines in the Mo base electrode appears to result from batch-to-batch variability in base electrode preparation.
- Significant progress has been made in understanding transient effects in CIS devices through independent studies at SSI and through participation in Thin Film Photovoltaic Partnership Program National CIS R&D Team. Transient effects are important for many topics including accelerated testing, process definition, measurement protocols, process predictability, interpretation of experimental test results, and understanding of device structures.
- The confounding of accelerated test results by transient effects in many ways delimits subcontract results for environmental studies. Confounding of test results makes drawing conclusions more difficult; however, transient effect issues are not encountered during normal operating conditions.
- Packaging designs that protect laminates from water vapor ingress during damp heat testing have been demonstrated and multiple prototype module designs have passed accelerated tests, including the 1,000 hour, 85°C, 85% relative humidity damp heat test. However, the yield for passing the damp heat test with these packages is typically low and improved package designs are required.
- Long term outdoor stability of CIS continues to be demonstrated at NREL where ~30x30 cm and ~30x120 cm modules have undergone testing for over ten years.
- SSI delivered two sets of upgraded modules for 1 kW arrays to the NREL Outdoor Test Facility. Improvements in efficiency and the temperature coefficient for power were demonstrated for these modules with sulfur incorporated to form a graded multinary ($Cu(In,Ga)(Se,S)_2$) absorber. The NREL measured average module efficiency at standard test conditions is 11.4 % for the second array, and the efficiency of all modules far exceeds the DOE year 2000 goal of 10% for commercial CIS modules.
- SSI demonstrated a succession of NREL confirmed world-record efficiencies culminating in demonstration of an 11.8 % efficient large area, 3651 cm^2, module.

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13. ABSTRACT *(Maximum 200 words)*
Siemens Solar Industries (SSI) achieved outstanding progress toward NREL/DOE goals during this subcontract. The statistical process control methodology was applied, and it demonstrated process reproducibility and yields for a 10-cm x10-cm substrate size baseline process. Based on an understanding of the importance of materials of construction and the physical layout for absorber formation reactors, SSI designed and built a replacement large-area reactor based on a more direct scale-up of the baseline reactor. While designing and building the new large-area reactor, SSI defined and demonstrated new package designs to combine 10-cm x 30-cm circuit plates into one package; this allowed SSI to deliver large-area prototype modules to NREL for evaluation, and to introduce the first CIS-based *products* – 5-watt (ST5) and 10-watt (ST10) modules. After completion of the new large-area reactor, all processes were scaled to a ~30-cm x 120-cm plate size. Subsequently, only large ~30-cm x 120-cm circuit plates were fabricated for ~30-cm x 120-cm prototype modules or, after cutting the large circuit plates into smaller circuit plates, for the two new CIS-based products. The scaled process exhibits generally good control for extended periods with periodic shifts in the short-term process average that appears to result from batch-to-batch variability in precursor or base electrode preparation. Similarly, periodic shunting along the laser-scribed pattern lines in the Mo base electrode appears to result from batch-to-batch variability in base electrode preparation. Significant progress was made in understanding transient effects in CIS devices. Transient effects are important for many topics, including accelerated testing, process definition, measurement protocols, process predictability, interpretation of experimental test results, and understanding of device structures. Long-term outdoor stability of CIS continues to be demonstrated at NREL where ~30-cm x 30-cm and ~30-cm x 120-cm modules have undergone testing for more than ten years. SSI delivered two sets of upgraded modules for 1-kW arrays to the NREL Outdoor Test Facility. Improvements in efficiency and the temperature coefficient for power were demonstrated for these modules with sulfur incorporated to form a graded multinary ($Cu(In,Ga)(Se,S)_2$) absorber. The NREL-measured average module efficiency at standard test conditions is 11.4% for the second array, and the efficiency of all modules far exceeds the DOE year 2000 goal of 10% for commercial CIS modules. SSI demonstrated a succession of NREL-confirmed world-record efficiencies culminating in demonstration of an 11.8 %-efficient, large-area, 3651-cm^2 module.

14. SUBJECT TERMS
photovoltaics ; Thin-Film Photovoltaic Partnership ; CIS-based thin films ; high throughput ; high-yield ; thin-film deposition ; high-performance modules

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